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A 94GHz TEMPERATURE COMPENSATED LOW NOISE AMPLIFIER IN 45nm SILICON-ON-INSULATOR COMPLEMENTARY METAL-OXIDE SEMICONDUCTOR (SOI CMOS)

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14. ABSTRACT
The objective of this proposal is to design and characterize components for utilization in a 94GHz temperature compensated low noise amplifier (LNA) using a 45nm SOI CMOS technology. A ring oscillator based temperature sensor will be designed to compensate for gain variations over temperature. For comparison to a competing solution, a temperature sensor will also be developed in 90nm CMOS to be utilized in conjunction with a III-V based 94 GHz LNA.

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SUMMARY

The objective of this work was to design and characterize components for utilization in a 94GHz temperature compensated low noise amplifier (LNA) using a 45nm silicon on insulator (SOI) complementary metal-oxide-semiconductor (CMOS) technology. A ring oscillator based temperature sensor was designed to compensate for gain variations over temperature. For comparison to a competing solution, a temperature sensor was also designed in 90nm CMOS to be utilized in conjunction with a III-V based 94 GHz LNA. The results corresponding to five listed tasks are summarized as following.

Task 1: Probe and characterize a 94GHz LNA in 45nm SOI technology. The measurements were completed at room temperature. The existing Air Force Research Laboratory (AFRL) probe station doesn't allow -55C to +125C operation. More resources are required to characterize across the complete temperature range.

Task 2: Design and characterize a temperature controlled oscillator. This task was completed in two technology nodes, namely 65nm CMOS and 45nm SOI technologies. The chip was tested in temperature chamber and the results were published in an Institute of Electrical and Electronics Engineers (IEEE) conference.

Task 3: Design of close-loop temperature compensated (TC) LNA in 45nm SOI. This task is completed with schematic and layout design. Simulation results show the close-loop operation. This design is ready for tape-out.

Task 4: Design the temperature controlled oscillator (TCO) in 90nm CMOS technology which is compatible with compound semiconductor materials on silicon (COSMOS) technology. This task is completed and the chip is delivered to AFRL.

Task 5: Build a W-band noise figure (NF) measurement system. This task is completed and verified in AFRL, and currently used to characterize a 94GHz LNA design in COSMOS technology.

By completion of this project, all the listed tasks have been accomplished with some extra features. The complete temperature characterization of LNA using wafer probe station was limited by existing equipment in AFRL. The principal investigator (PI) participated two terms of Air Force Summer Faculty Program. This activity significantly helped in the completion of the tasks listed in this grant. During the period of this project, the PI and the supported students presented one paper in the NAECON (National Aerospace & Electronics Conference) 2011 conference and one paper in the 54th IEEE International Midwest Symposium on Circuits and Systems, together with one paper in 2013 International Symposium of Quality Electronics Design (ISQED).

The detailed description and measurement results are arranged as follows. Chapter 1 gives an introduction of this project. The design overview of LNA and temperature sensor are described in Chapter 2. In Chapter 3, the measurement results of 94GHz LNA are shown, the temperature sensor design and characterization results are discussed, and the concept of the close-loop

operation is discussed. Conclusions and Recommendations are described in Chapter 4 and Chapter 5, respectively.

1 INTRODUCTION

1.1 Background

Nano-scale CMOS technologies have enabled the cost effective implementation of many millimeter wave applications such as wireless high-definition multimedia interface (HDMI), automotive radar and passive imaging systems. While the CMOS realization of 60GHz radios [1-3] is drawing wider attention, similar efforts for passive imaging and W-band automotive radar have attracted researches in recent years [4-5]. The 94GHz passive imaging system has wide application in concealed weapon detection, homeland security, radio astronomy and medical imaging. Traditionally, the III-V devices and silicon germanium (SiGe) devices are employed for 94GHz imaging systems. As the CMOS technology scaling to nano-scale, it is feasible to realize those millimeter wave system using CMOS devices for the sake of low cost and high level of integration with complex baseband.

As the first stage of the receiving chain, the LNA often limits the receiver performance. The LNA is also used to benchmark the performance of a technology. The Defense Advanced Research Projects Agency (DARPA) COSMOS program is to develop a viable process for the fine-scale heterogeneous integration of compound semiconductor (CS) devices with standard Si CMOS and to establish that this integration enables superior performance in specific mixed-signal circuit demonstrators. The LNA is also used in COSMOS program to bench mark the performance improvement. By comparison of the COSMOS LNA and the state-of-the-art CMOS LNA, design insights can be achieved for the noise, gain, linearity and power performance trade-off.

Meanwhile, the demand for smart temperature sensors keeps growing in very-large-scale integration (VLSI), wireless, automotive and biomedical applications. The possibility of constantly monitoring the chip temperature plays a key role on long-term system reliability and performance and, due to the increasing transistor number per die, low area and low power sensors are required, to be spread over the chip and manage the temperature of different areas. That’s because the total area occupation of the sensors shouldn’t greatly affect the circuit dimensions, break the power grid integrity, or increase the heating problem.

1.2 Approach

Several works have been done in that direction, differentiating for their trade-off between area, power consumption, temperature range and accuracy.

The most common and simple design measures either a voltage or a current proportional to the difference between the base-emitter voltages of two bipolar junction transistors (BJTs), differently biased with a precise current ratio that is proportional to absolute temperature (PTAT). However, due to process spread, such sensors can’t get accuracy less than a few degrees Celsius; only by calibrating and trimming each individual circuit can be reduced. Obviously that is at the expense of the increased manufacturing cost and time. Another limitation in such an approach is the use of bipolar transistors. Especially in the nano-era, the fabrication process and the device scaling are moving and specializing only in the direction of the metal-oxide-semiconductor field-effect transistor (MOSFET), leaving behind the old BJT technology, considered to have the same level of performance and possible improvement.

Meanwhile, in the work reported in [6], the temperature sensor consumes 190 μW and occupies an area of 4.5 mm^2, obtaining an inaccuracy of ±0.1 °C over the very wide range of -55 °C ~ 125 °C. Some researchers have then tried to find alternative ways and components to achieve better results, such as thermocouples, resistance temperature devices (RTDs), bimetallic and liquid expansion devices. For instance, in [7] is presented the original idea of building on the silicon an electro-thermal filter combining an n^+ diffusion resistor with some p^+ diffusion/aluminum thermocouples. That structure behaves like a filter, introducing a well defined temperature-dependent phase shift. Measuring that, they have achieved a sensor working between -40 °C and 105 °C, with an inaccuracy of ±0.5 °C and occupying an area of 2.3 mm^2; dissipating 2.5 mW though. However, the construction of a thermocouple on the silicon is a thorny issue, because it is not a component that the foundry usually builds. So the design and the modeling of that part is completely left to the engineer, increasing the probability of circuit fault, the fabrication time and, as a result, the cost. Thus, that kind of temperature sensor is not suitable for large scale production or integration.

To minimize as much as possible the sources of measurement inaccuracy, most of the recent works use a bandgap to obtain a reference voltage independent from the temperature variation [8], as in this work and in [9]. They have used the 0.18 μm CMOS technology to implement a system quite similar to ours, transforming the temperature dependence of an I_{PTAT} current into a temperature dependent frequency using a ring oscillator. Comparing that to a temperature independent frequency generated by a similar circuit using a reference current, they have reached a 220 nW sensor in the range of 0 °C ~ 100 °C, with an occupation of 0.05 mm^2 and an inaccuracy of -1.6/+3 °C. Using that technique, they have found a way to obtain an automatic calibration, independent from the process corners, that makes the system an optimum choice for a mass production, because there is no need to probe every single chip after the fabrication. The drawbacks are the area occupation and the power consumption, because everything is doubled inside the chip. There is also a crucial aspect that has to be noticed: they are driving a ring oscillator that decreases its frequency with the increasing of the temperature, by an I_{PTAT} current. Following the intrinsic characteristic of the oscillator, they should have used a current inverse proportional to the absolute temperature. Thus that can be considered a bad solution.

Nevertheless, the designs exploiting the delays of inverts are really suitable for microprocessor applications, as they lend themselves to a digital and low-power implementation; so the trend is moving in that direction. Also in [10] authors compare the delay of two ring oscillators, one of them calibrated based on the process variations, introducing an interesting idea though: performing a series of temperature measurements and calculating their average to obtain the final result with a better accuracy. This will lead to a higher power consumption and time per complete measurement, while the right trade-off is application specific.

Based on the on-chip CMOS temperature sensor and millimeter wave low noise amplifier, the PI proposed to design temperature compensated low noise amplifier circuitry using an optimal compensation algorithm. The trade-off between the calibration accuracy and the gain control accuracy can also be revealed by this investigation.

1.3 Scope

The scope of the report is organized as follows: Chapter 2 gives an introduction of this work, Chapter 3 describes details of 94GHz LNA design, temperature sensor design, and the concept of

close-loop operation. Chapter 4 draws the conclusion. In Chapter 5, recommendations of continuing this work in both the design and characterization are given.

2 DESIGN OF TEMPERATURE COMPENSATED LOW NOISE AMPLIFIER

Two key components of this project are the design, implementation and characterization of a 94GHz LNA in 45nm SOI CMOS, together with a ring-oscillator based CMOS temperature sensor either on 45nm CMOS or 90nm CMOS which is compatible with COSMOS technology.

2.1 94GHz Low Noise Amplifier in 45nm SOI CMOS

This report includes the design, implementation and test of a 94GHz low noise amplifier using 45nm SOI CMOS technology. Fig. 1 shows the simplified circuit diagram of the proposed three-stage single-ended LNA. The optimization of the different stages has been performed according to the methodology proposed in [11]. The common source transistors of the first and second stages consist of M_1 and M_2. The cascode configuration (M_3 and M_4) is utilized in the third stage to achieve high gain performance. To improve the gain and noise performance of the third stage, the parasitic capacitance at the drain of transistor M_3 is resonated by adding a series inductor between the source of transistor M_4 and drain of transistor M_3. To protect against electrostatic discharge (ESD) stress the high-pass input matching network, designed for minimum noise figure, has been modified by adding an extra ESD coplanar waveguide (CPW) transmission line at the input of the LNA, between the radio frequency (RF) signal path and groupnd (GND), forming a high-pass pi-matching network. The length of the CPW transmission line is chosen in such a way that the parasitic inductor of the CPW transmission line resonates with the parasitic capacitance of the RF pad at the frequency of operation. Therefore, the capacitive loading effect of the RF pad is minimized and ESD protection is provided at the same time. The values of the other elements of the input matching network are dimensioned for minimum noise figure.

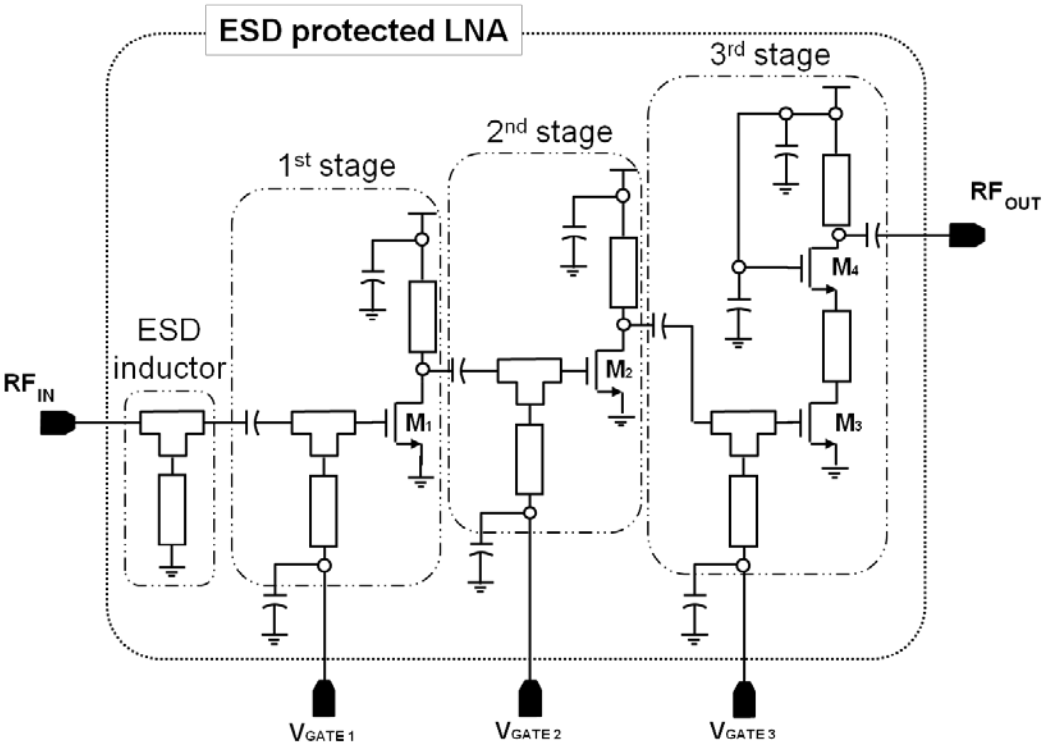


Figure 1: Simplified Schematic Diagram of Proposed 94GHz Low Noise Amplifier

2.2 Ring Oscillator Based Temperature Sensor

The main idea behind the proposed temperature sensor design is to convert the temperature into a frequency reference, easier to be evaluated in a CMOS circuit, achieved thanks to a TCO. Fig. 2 shows the block diagram of our system. As you can see, in addition to the TCO, we need a voltage regulator, a counter, a register, a subtractor and a parallel-to-series converter.

The voltage regulator is used to provide the TCO with a supply voltage always constant over the temperature, thanks to its internal bandgap reference. Without it, the measurement would be affected also by that source of error, because the oscillator modifies its frequency also depending on the applied voltage; but our intent is to have an output frequency that can only be related to the temperature value.

The counter has the purpose to transform the frequency information of the TCO into a bit code, simply counting the number of oscillation pulses over a predetermined period of time.

The counter output value at the temperature at which we want to calibrate the sensor is stored in the 15-bit register. At the end of each counting period, the subtractor will perform the subtraction between the counter output and the register value. In that way, the output bit code basically establishs the distance between the calibration temperature and the actual one. That helps obtaining a better accuracy around the calibration temperature and a less number of bits for the dynamic range of the code.

The final block is simply a parallel-to-series converter. We have implemented it because, in a chip, it is better to provide as output a sequence of bits using a single pad than 15 bits in parallel that require 15 pads, especially when the chip is pad limited due to its small dimensions.

The whole system is controlled by the *Enable* and the *Measure_Temperature* signals. First of all the former has to be provided to start up the circuit; then, when the oscillator has reached its steady state, the latter has to be set high during the desired period of counting. The system can be put in sleep mode by setting both low, in order to consume the minimum power.

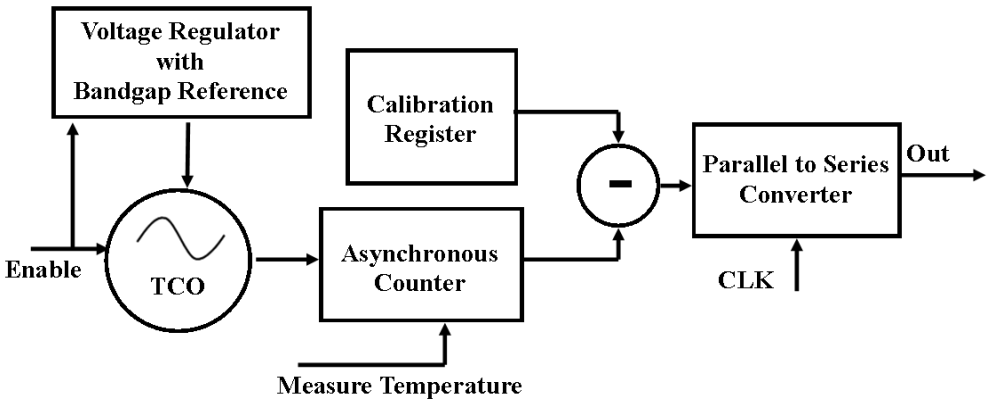


Figure 2: Temperature Sensor Block Diagram

3 RESULTS AND DISCUSSION

This chapter discusses results of the components and circuits of the 94GHz LNA, ring oscillator based temperature sensor and noise figure measurement setup based on the Y-factor method.

3.1 94GHz LNA Results

This section discusses specific results of 94GHz LNA in 45nm SOI CMOS, namely the pad, transmission line, capacitor, single transisitor, single-stage LNA and two-stage LNA.

3.1.1 Chip Overview

The die diagram of the chip is shown in Fig. 3. It consists of 8 different circuits or components: one 2-stage LNA, one single-stage LNA, one single N-type metal-oxide-semiconductor (NMOS) device, one on-chip capacitor, one L and one 2L coplanar waveguides, one TCO, and one transceiver. All the circuits have been tested and measured in the AFRL facility.

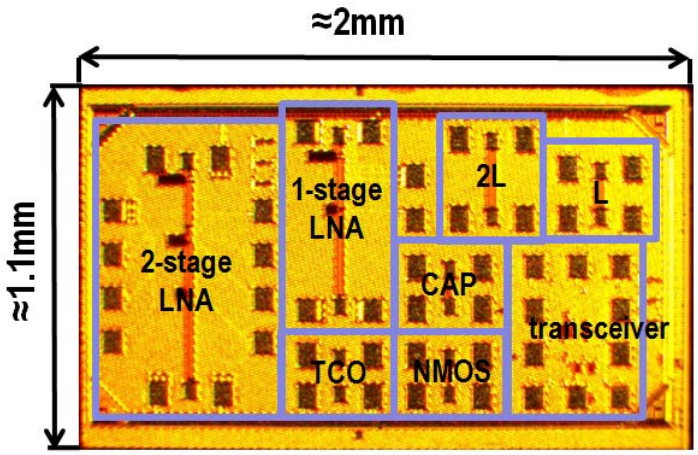


Figure 3: Die Micrograph (IBM 45nm SOI)

3.1.2 GSG Pad Measurements

The full S-parameters of the ground-signal-ground (GSG) pad have been calculated through the L-2L deembedding technique. Fig. 4 shows those results. The dotted line corresponds to the simulated values, while the solid line correspond to the measured values.

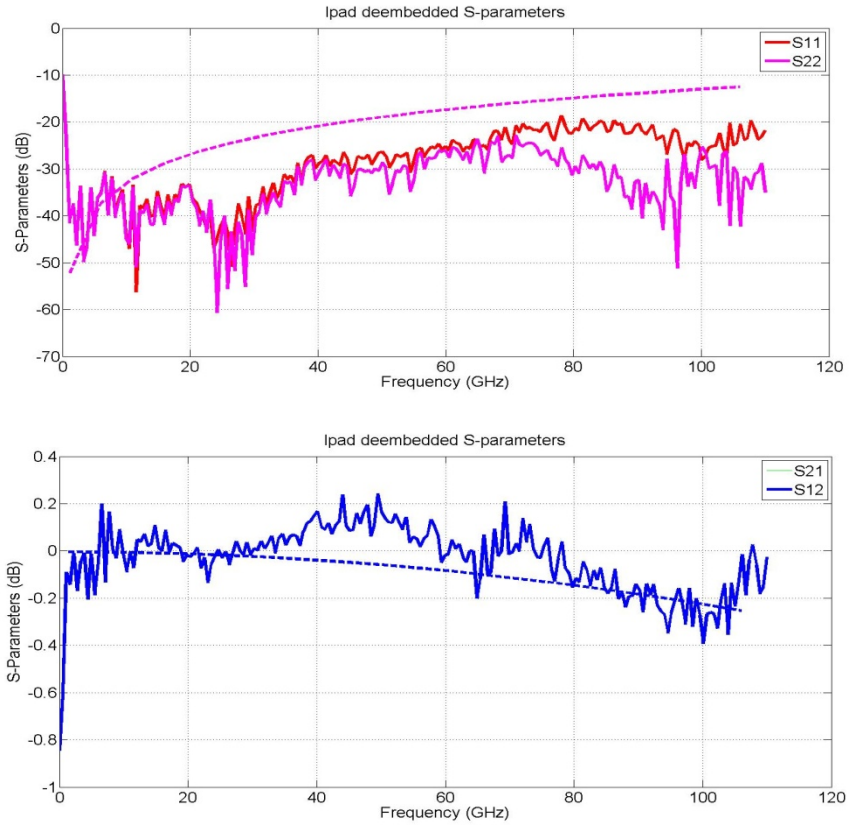


Figure 4: Measured (Solid) and Simulated (Dotted) S-parameters for the GSG Pads

The corresponding capacitance of the pad is shown in Fig. 5. It can be observed how the measured capacitance (blue line) is about half of the simulated red capacitance (green line).

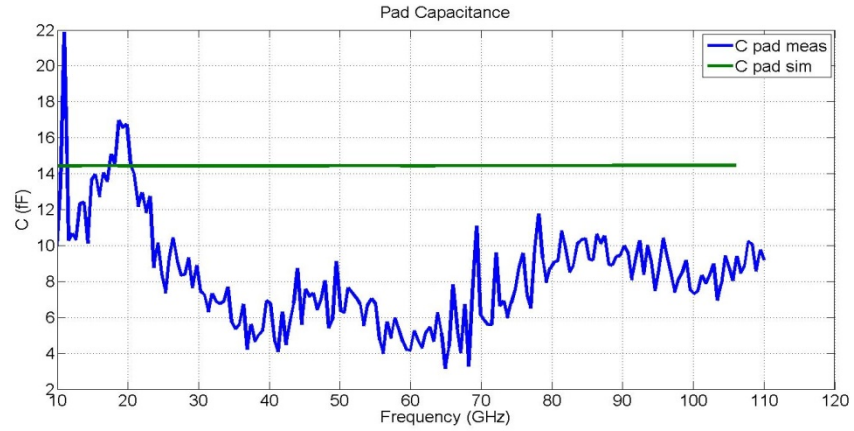


Figure 5: Measured (Blue) and Simulated (Green) Capacitance of the GSG Pads

3.1.3 L - 2L Coplanar Waveguide Measurements

Fig. 6 shows the die picture and the schematic of the two coplanar waveguides used for the L–2L deembedding technique. Setting down the RF probes, the full S-parameters have been measured between 1GHz and 110GHz. The results for the L and the 2L coplanar waveguides including the GSG pads are shown respectively in Fig. 7 and Fig. 8.

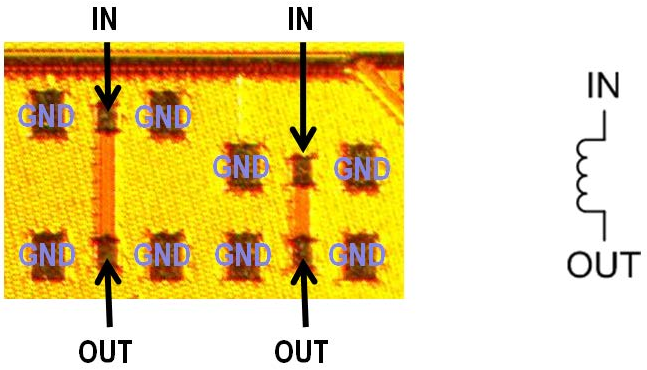


Figure 6: Die Picture and Schematic of the L-2L Coplanar Waveguides

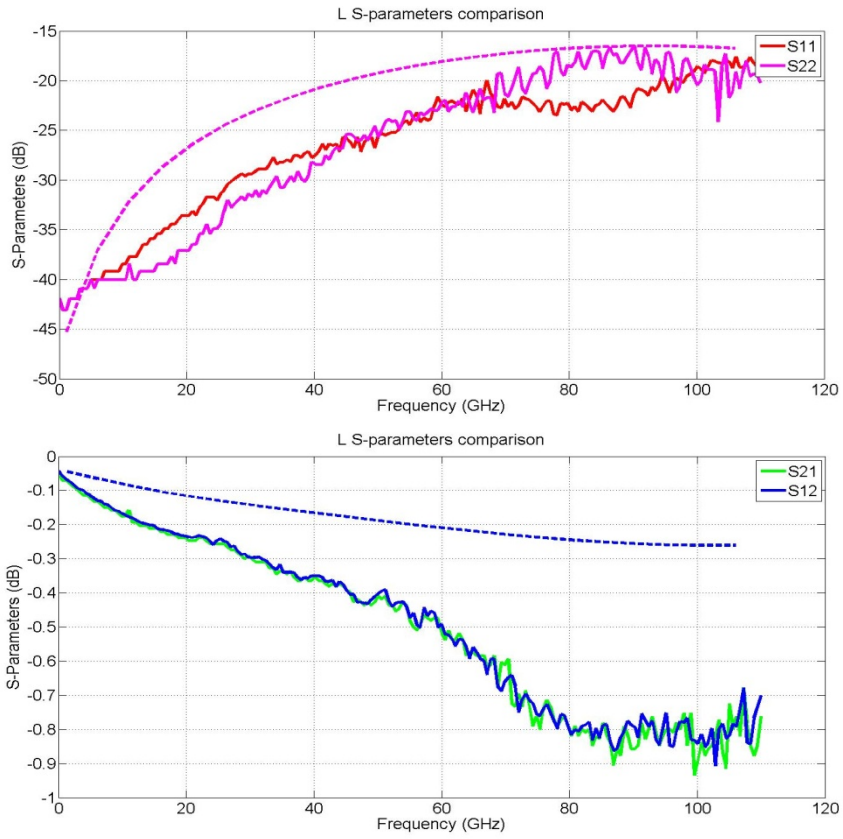


Figure 7: Measured (Solid) and Simulated (Dotted) S-parameters of the L CPW Including GSG Pads

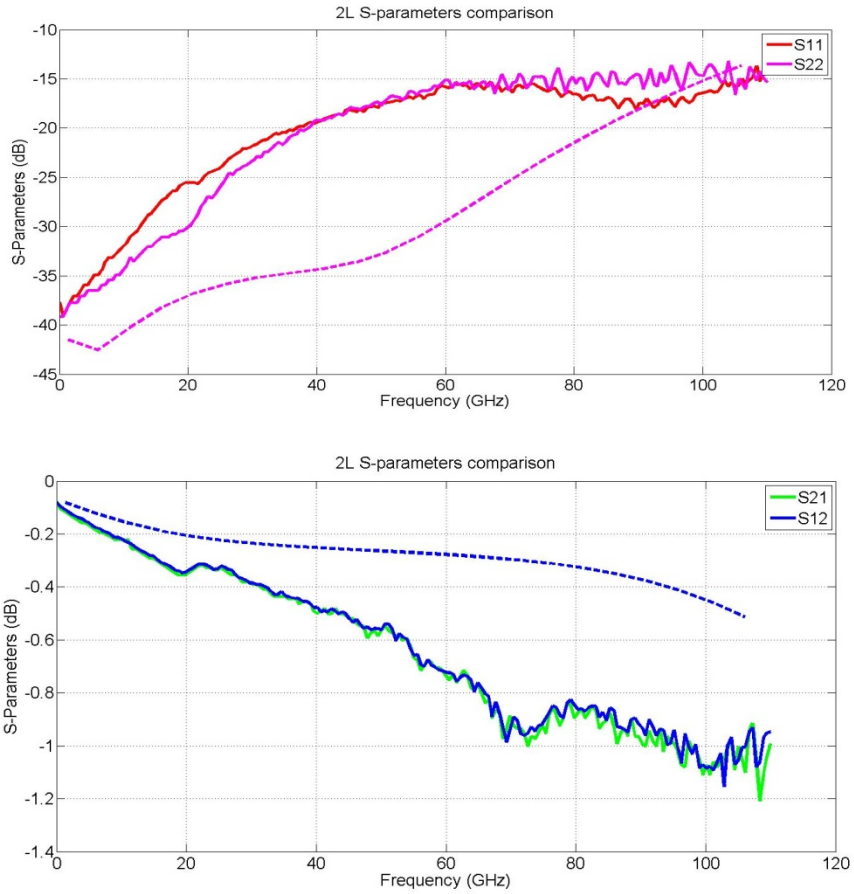


Figure 8: Measured (Solid) and Simulated (Dotted) S-parameters of the 2L CPW Including GSG Pads

The S-parameters for the L and 2L CPWs by themselves, after performing the L-2L deembedding technique, are shown respectively in Fig. 9 and Fig. 10.

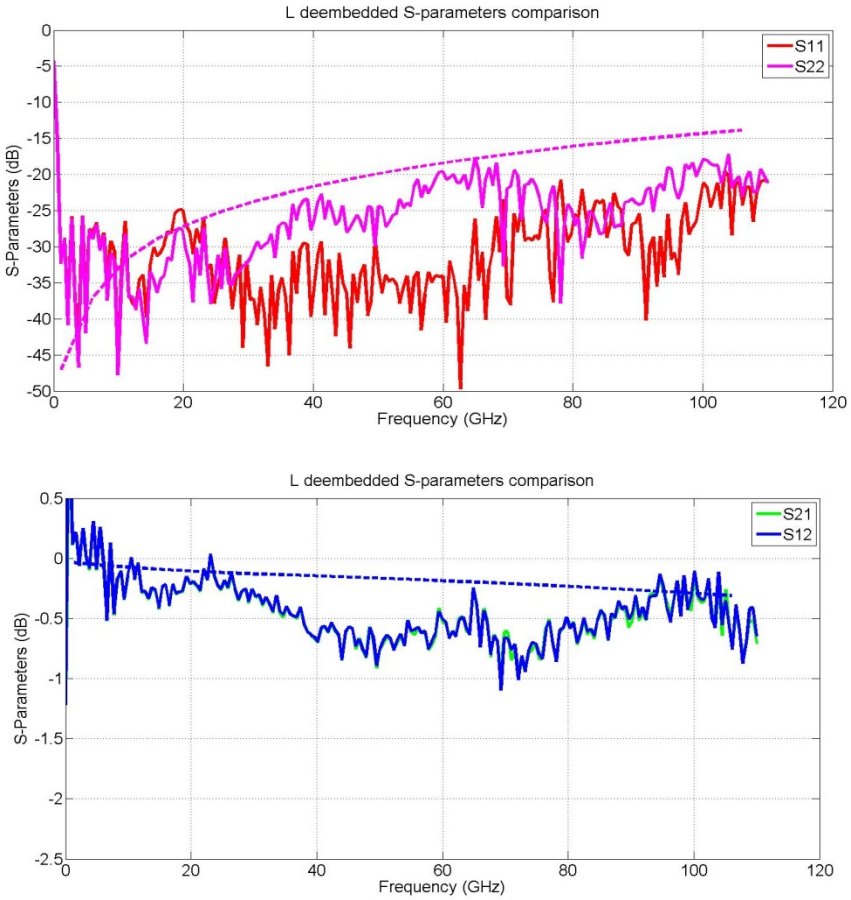


Figure 9: Measured (Solid) and Simulated (Dotted) S-parameters of the Deembedded L CPW

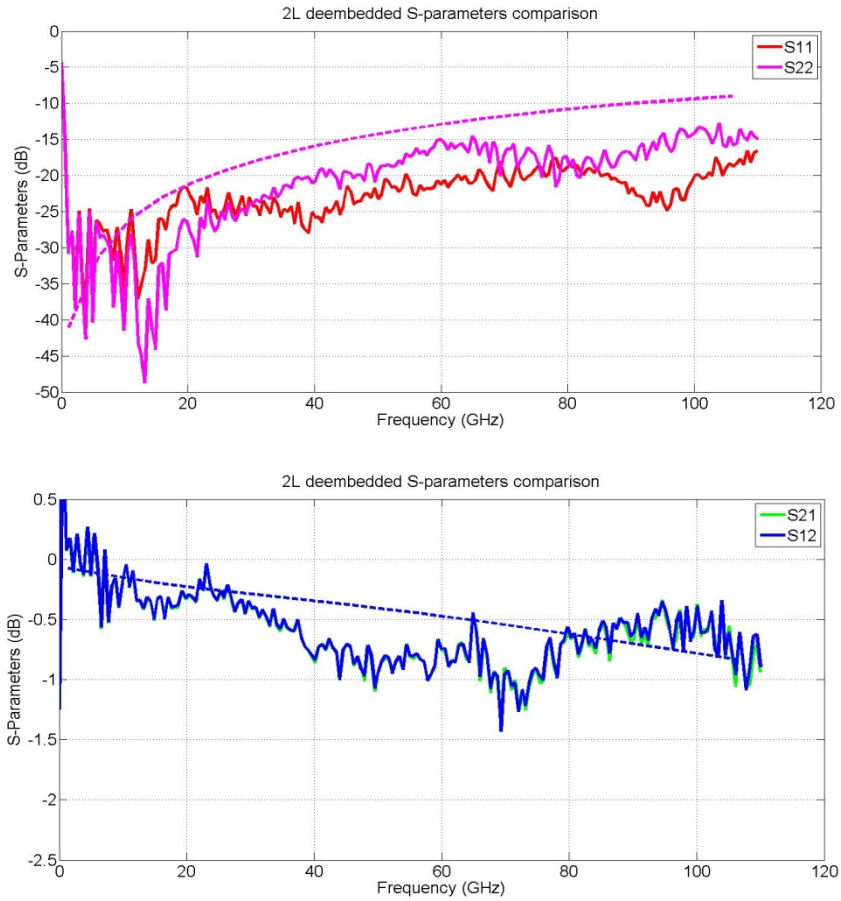


Figure 10: Measured (Solid) and Simulated (Dotted) S-parameters of the Deembedded 2L CPW

From the deembedded S-parameters, the inductance and the quality factor for the the L and the 2L CPWs have been derived and are shown in Fig. 11 and Fig. 12. It can be observed how the measured inductance is about 20% lower than the simulated one. At the same time the measured quality factor is extremely lower than the simulated one.

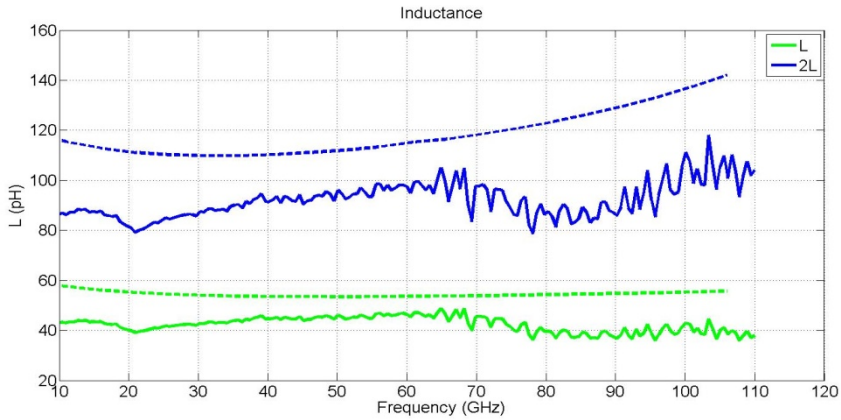


Figure 11: Measured (Solid) and Simulated (Dotted) Inductance of the L and 2L CPWs

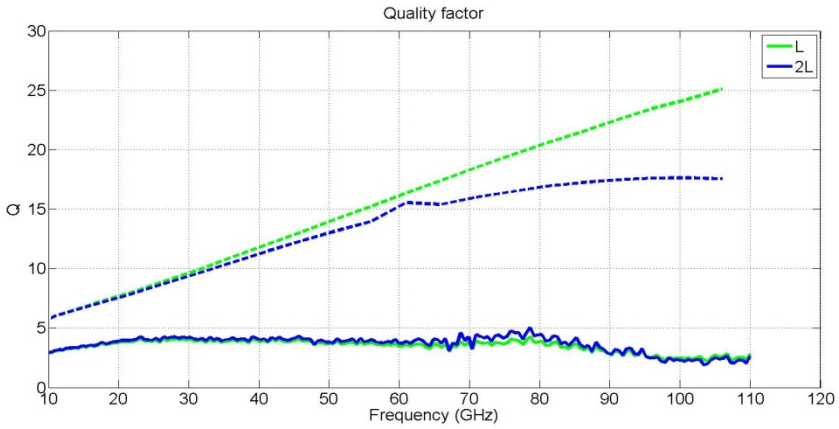


Figure 12: Measured (Solid) and Simulated (Dotted) Quality Factor of the L and 2L CPWs

3.1.4 On-Chip Capacitance Measurements

Fig. 13 shows the die picture and the schematic of the on-chip capacitance. Setting down the RF probes, the full S-parameters have been measured between 1GHz and 110GHz. The results are shown in Fig. 14. The difference between the measured and simulated S-parameters is due to the pad model. Fig. 15 shows the capacitor S-parameters after having deembedded the pads.

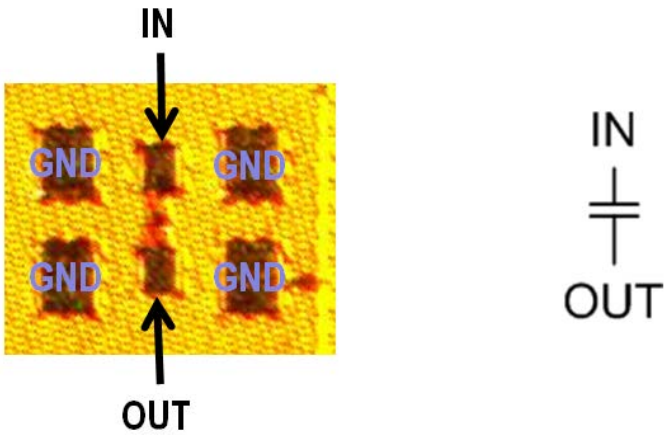


Figure 13: Die Picture and Schematic of the On-chip Capacitance

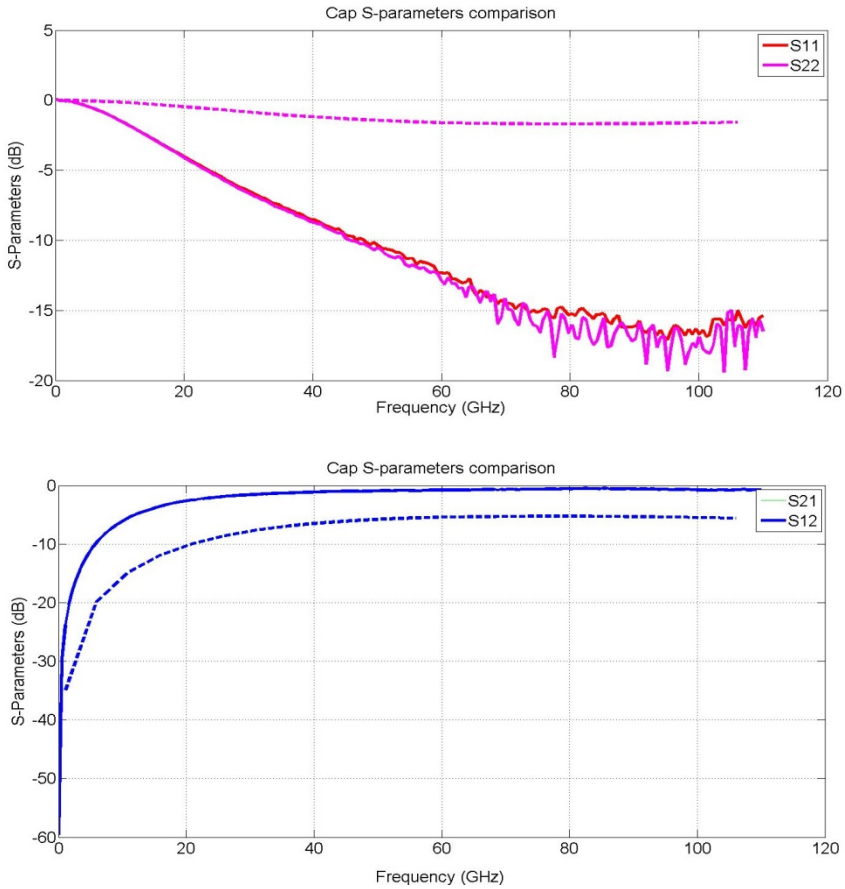


Figure 14: Measured (Solid) and Simulated (Dotted) S-parameters of the On-chip Capacitor Including GSG Pads

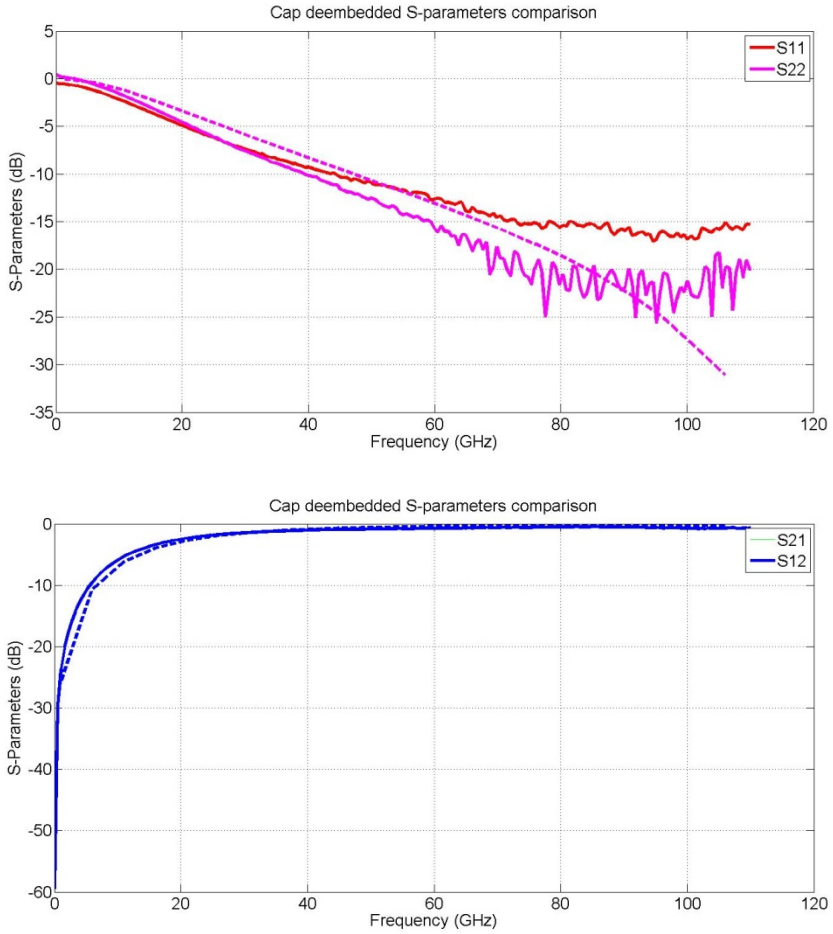


Figure 15: Measured (Solid) and Simulated (Dotted) S-parameters of the deembedded On-chip Capacitor

From the deembedded S-parameters, the capacitance of the on-chip capacitor has been derived as shown in Fig. 16. The measured capacitance value is in accord with the simulated one. The resonance that can be observed in the capacitance plot is due to the inductance of the connections between the capacitor and the GSG pads.

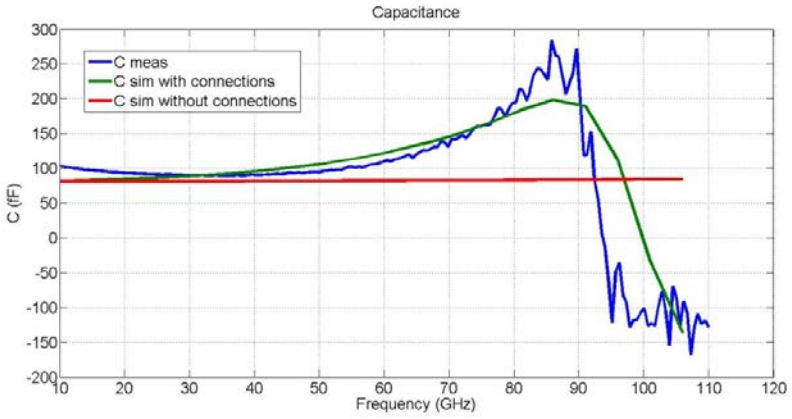


Figure 16: Measured (Blue) and Simulated (Green) Capacitance of the On-chip Capacitor

3.1.5 Single NMOS Device Measurements

Fig. 17 shows die image of the single NMOS devices and a corresponding schematic. First the I-V direct current (DC) characteristic of the device has been measured based on the following procedure.

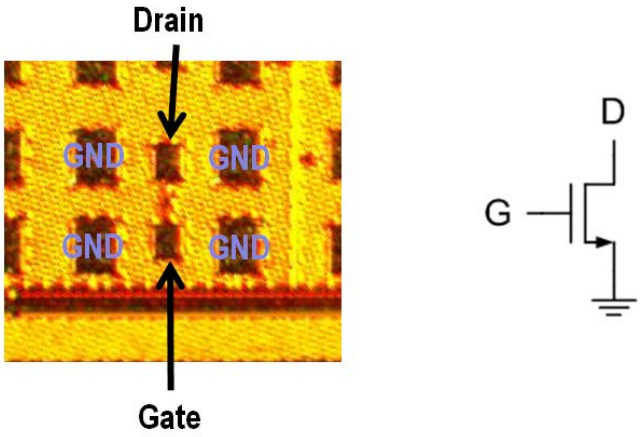


Figure 17: Die Picture and Schematic of the Single NMOS Device

Step 1: set down the GSG probes for gate and drain.

Step 2: set the gate DC voltage to 0.45V.

Step 3: sweep the drain DC voltage from 0V to 1.2V, steps of 10mV.

Step 4: measure and record the drain current at each step.

Step 5: repeat the procedure for gate DC voltage equal to 0.5V, 0.55V, 0.6V, 0.65V.

The DC results are shown in Fig. 18. The solid line corresponds to the measured value, while the dotted line corresponds to the simulated values.

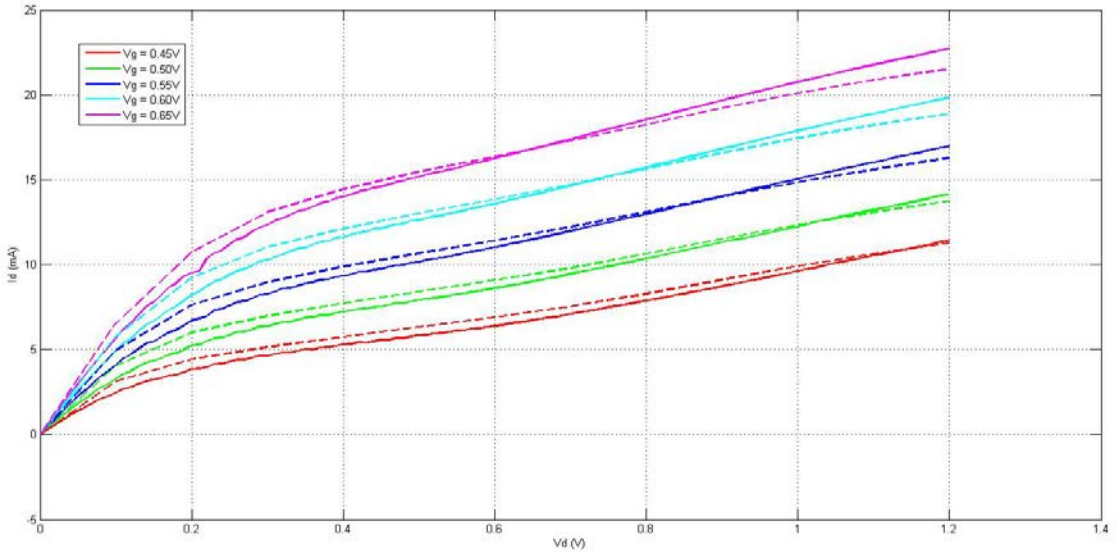


Figure 18: I-V Characteristic of the Single NMOS Devices

Next the device S-parameters have been measured between 1GHz and 110GHz. Fig. 19 shows the measured results for Vg = 0.55V and Vd = 0.5V. The difference between the measured and simulated S-parameters is due to the pad model. Fig. 20 shows the NMOS S-parameters after having deembedded the pads. The solid lines represent measurement results, while the dotted lines represent simulated results. The dotted line with markers represents simulated results without including the inductance of the connections between the device and the GSG pads. It can be observed how the inductance of the connections has to be taken into account in order to match the simulated and measured S22. That means the output match is really sensitive to small inductance changes in the load.

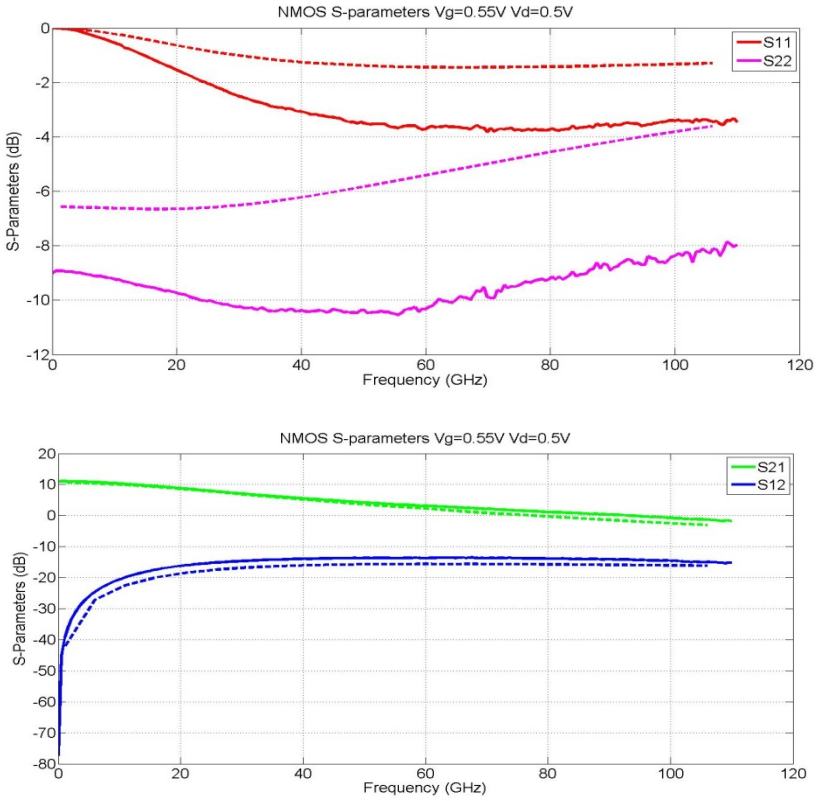


Figure 19: Measured (Solid) and Simulated (Dotted) S-parameters of the NMOS Device Including GSG Pads

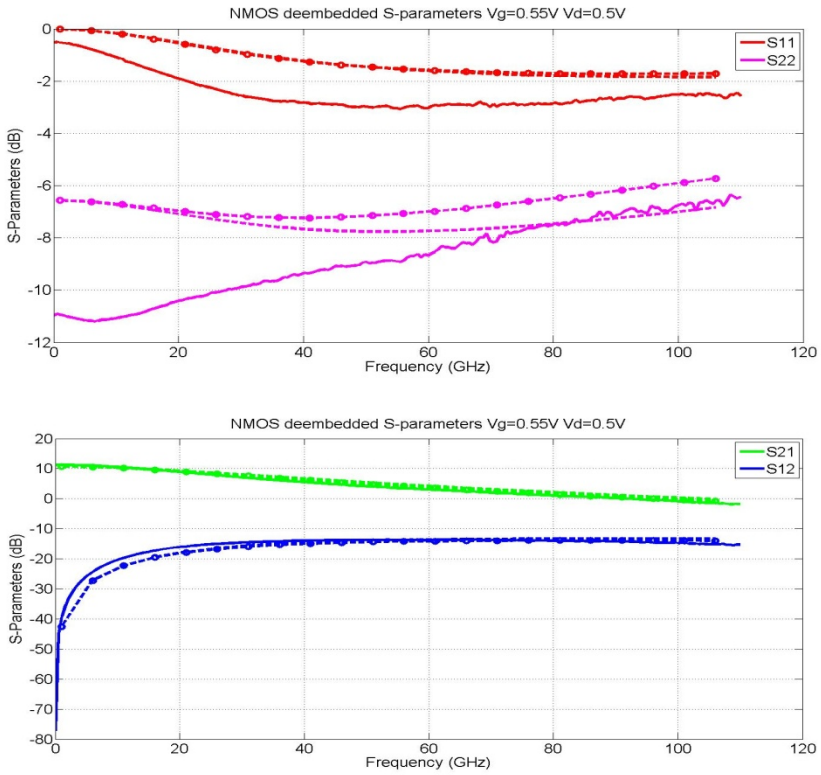


Figure 20: Measured (Solid) and Simulated (Dotted) S-parameters of the NMOS Device

3.1.6 Single-stage 94GHz LNA Measurements

Fig. 21 shows the die picture and the schematic of the single-stage 94GHz LNA. The DC bias operating point has been established based on the following procedure.

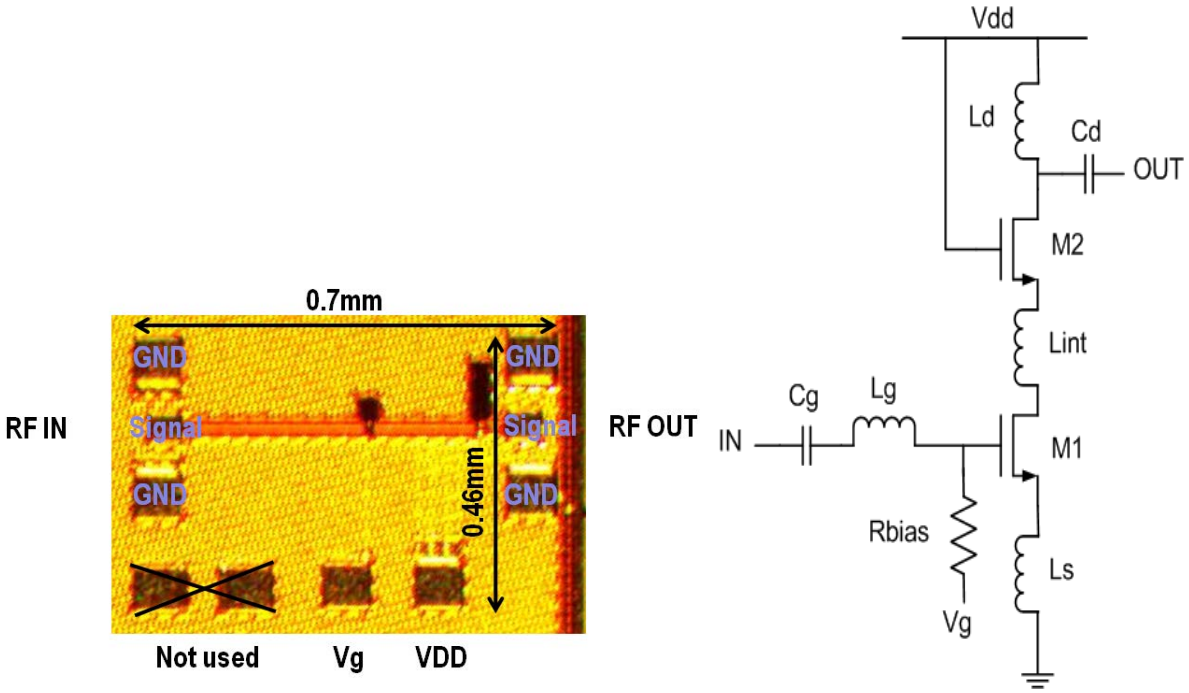


Figure 21: Die Picture and Schematic of the Single-stage LNA

Step 1: set the current and voltage limits in the power supplies to 15mA and 1.1V respectively.

Step 2: set supplies for Vdd = 0V and Vg = 0V (all OFF).

Step 3: set RF probes down for grounding.

Step 4: set down the bias probes to corresponding pads.

Step 5: turn ON the power supplies while at 0V.

Step 6: slowly increase Vdd to 1V.

Step 7: slowly increase Vg until the Vdd current is 10mA (approximately 550mV).

Then the full S-parameters of the 1-stage LNA have been measured and the results are shown in Fig. 22. The gain dropped from the expected value of 6dB because of the extremely low Q of the coplanar waveguides provided by the process design kit (PDK). The output match shifted to a lower frequency because the inductance of the connection between the output load and the VDD pad hasn't been accounted for. The critical connection is shown in Fig. 23 where you can see the layout of the LNA. Taking into account the low Q and the inductance of the critical connection, the simulation matches the measured results.

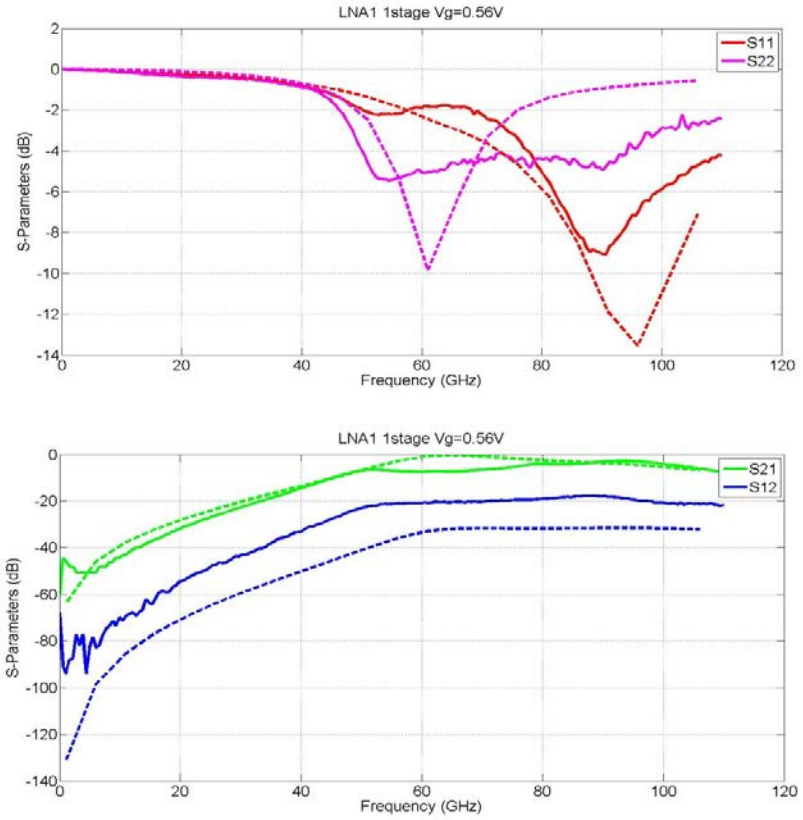


Figure 22: Measured (Solid) and Simulated (Dotted) S-parameters of the 1-stage LNA

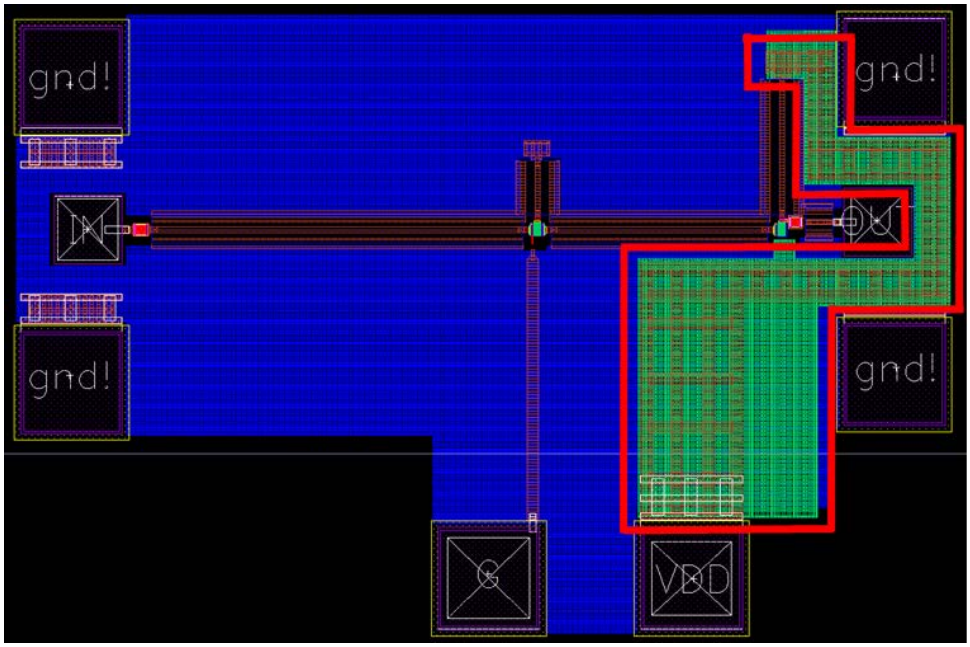


Figure 23: Layout of the 1-stage LNA
The critical connection is highlighted in red

3.1.7 Two-stage 94GHz LNA Measurements

Fig. 24 shows the die picture and the schematic of the single-stage 94GHz LNA. The DC bias operating point has been established based on the following procedure.

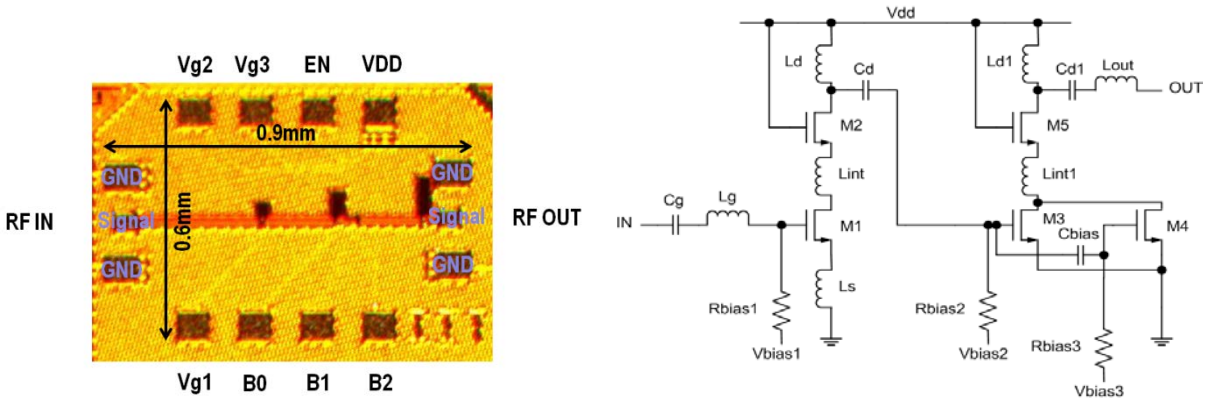


Figure 24: Die Picture and Schematic of the 2-stage LNA

Step 1: set the current and voltage limits in the power supplies to 25mA and 1.1V respectively.

Step 2: set the supplies for Vdd, EN, B0, B1, B2, Vg1, Vg2 and Vg3 to 0V (all OFF).

Step 3: set the RF probes down for grounding.

Step 4: turn ON all the power supplies while at 0V.

Step 5: connect Vdd, B0, B1, B2 using the same power supply and slowly increase it to 1V.

Step 6: connect Vg1, Vg2 and Vg3 to the same power supply and slowly increase it until the Vdd current is about 22mA (approximately 550mV).

Then the full S-parameters of the 2-stage LNA have been measured and the results are shown in Fig. 25. The gain dropped from the expected value of 14dB to 8dB because of the not expected extremely low Q of the coplanar waveguides provided by the PDK. The output match shifted to a lower frequency because the inductance of the connection between the output CPW of both the stages and the VDD pad hasn't been accounted for. The critical connection is shown in Fig. 26 where you can see the layout of the LNA. Taking into account the low Q and the inductance of the critical connection, the simulation matches the measured results.

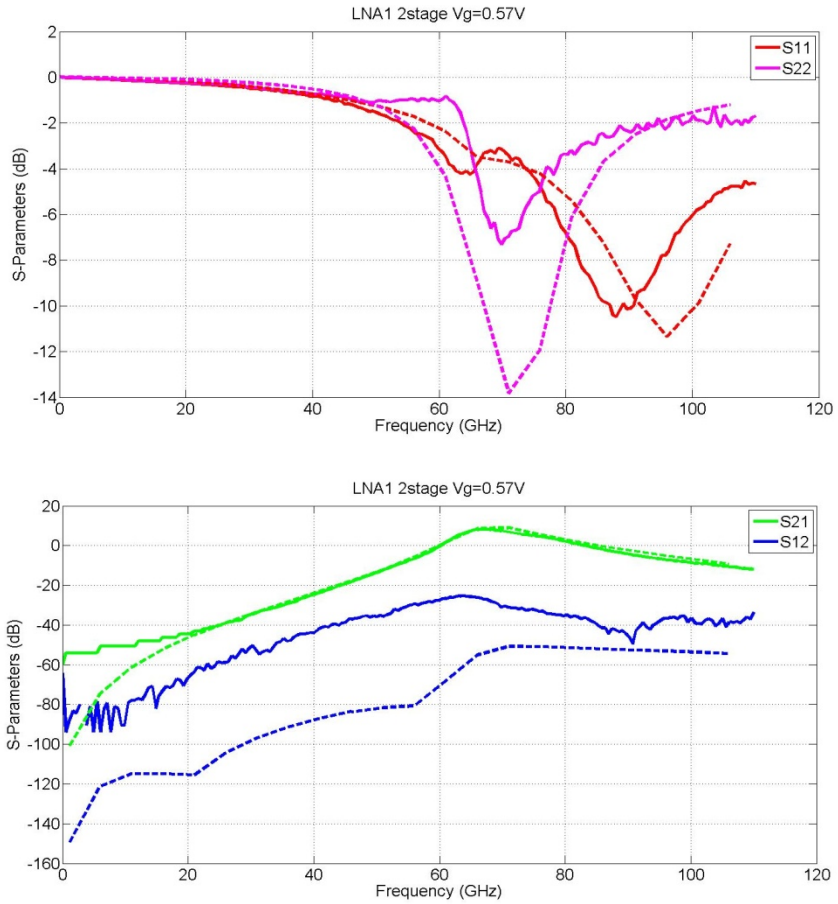


Figure 25: Measured (Solid) and Simulated (Dotted) S-parameters of the 2-stage LNA

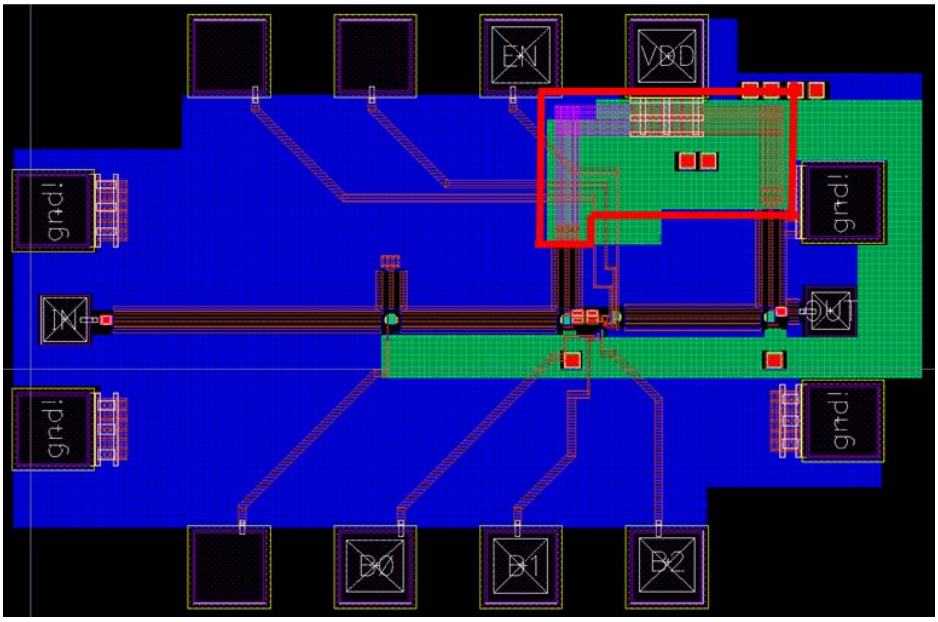


Figure 26: Layout of the 2-stage LNA
The critical connection is highlighted in red

3.2 Temperature Sensor Results

The demand for smart temperature sensors keeps growing in VLSI, wireless, automotive and biomedical applications. Constantly monitoring the chip temperature could play a key role on long-term system reliability and performance. Due to the increasing transistor number per die, temperature sensors with low area and low power are required, to be spread over the chip and manage the thermal profile of different sectors. The area occupied by the sensors shouldn't significantly affect the total chip area; while they shouldn't break the power grid integrity and exacerbate the heat problem.

Significant research has been conducted in this field, resulting in different sensing principles and circuit implementations, and leading to different trade-offs in area, power consumption, temperature range and accuracy. The most common temperature sensor measures a voltage or a current proportional to the difference between the base-emitter voltages of two BJTs, differently biased with a precise current ratio. That results in a voltage that is PTAT [6] [7]. However, due to process variation, such sensors can't get an inaccuracy less than a few degrees Celsius. Only by calibrating and trimming each individual circuit this can be reduced. Obviously it is at the expense of increased manufacturing cost and time. Meanwhile, researchers have tried to find alternative ways to achieve better results, such as RTDs [12] and bimetallic [13] devices. For instance, in [8] the original idea of building an on-silicon electro-thermal filter is presented. Combining a n+ diffusion resistor with some p+ diffusion/aluminum thermocouples, the structure behaves like a filter, introducing a well defined temperature-dependent phase-shift. Measuring that shift a sensor working between -55°C and 125°C with an inaccuracy of ±0.2°C has been achieved. The drawback is that the construction on silicon of this kind of structures and devices is not something commonly built by the foundries. Thereby their design and modeling is completely left to the engineers, increasing the design iterations and prolonging product cycles. Most of the recent works use a bandgap to obtain a reference voltage independent from temperature variations [9], to minimize as much as possible the sources of measurement inaccuracy. In [10], a 0.18 μm CMOS technology has been used to transform the temperature dependence of a PTAT current into a temperature-dependent frequency using a ring oscillator. Then it compares it to a temperature-independent frequency, using a reference current. In that way, a controller that compensates process variations is created, but the area and the power needed by the circuit are nearly doubled due to the comparison. The designs exploiting inverter delays are suitable for microprocessor applications, as they lend themselves to a digital and low-power implementation. In [14] the delays of two ring oscillators, one of them calibrated based on process variations, are also compared, but the concept of averaging is introduced in order to reduce the inaccuracy. That is an effective method, but it incurs extra power consumption.

In this work, the inaccuracy of the ring oscillator based temperature sensor is modeled by taking the phase noise into account, in order to reduce the single measurement error and avoid the averaging process. It also exploits the potential of nano-scale CMOS technology to implement a low area and energy efficient design with nano-Joule energy consumption.

3.2.1 System Architecture

This temperature sensor design converts the temperature information into a frequency reference, easier to be evaluated in a CMOS circuit. Fig. 27 shows the block diagram of the entire system. The TCO is the core element that performs the desired conversion. Its output oscillation frequency is directly proportional to the substrate temperature. An asynchronous counter is implemented to transform the oscillation frequency information into a binary code. The circuit is active only for a precise period of time *t* imposed by the *Measure Temperature* control signal. Its output represents the number of oscillations occurred during that time frame. The number of bits determines the resolution of the system: for a higher number of bits, *t* can be longer, so the differences in the output binary code between two close spaced frequencies, representing two close temperatures, are enhanced. At the same time, a longer *t* means higher power consumption. The number of bits is chosen to ensure several trade-off possibilities during testing: not all the bits have to be used every time, if the resolution is sufficient for the target application and power needs to be saved. Since the sensor should then be placed into bigger systems that could use different voltages, a voltage regulator has been designed. It provides the TCO with a supply close to 1V when the system VDD is between 1V and 1.2V. Using a built-in bandgap reference similar to [15], the regulator provides a stable voltage across the sensor temperature range. Those two features are extremely important since the TCO oscillation frequency strongly depends on its supply value.

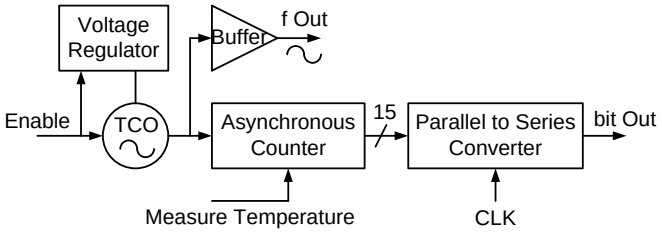


Figure 27: Temperature Sensor Block Diagram

The control signals *Enable* and *Measure Temperature* are used to activate or switch-off different blocks of the system, in order to save power when a temperature measurement is not needed. *Enable* wakes up the voltage regulator together with the TCO. After few nanoseconds the oscillation is stable and the *Measure Temperature* signal can activate the counter to obtain the final temperature value. After having read the data out, both the signals can go to zero and the system goes to sleep.

For the ease of testing, the chip includes a buffer to drive the 50Ω input of the spectrum analyzer, in order to read the TCO frequency, and a parallel-to-series converter, to not have many output pins.

3.2.2 Temperature Controlled Oscillator

In Fig. 28, a simplified schematic diagram of the TCO is shown.

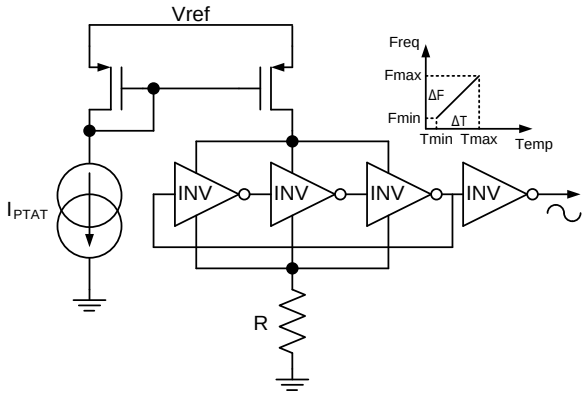


Figure 28: TCO Block Diagram

It consists of a 3-stage ring oscillator controlled by a PTAT improved cascode current source [16]. In that way, in a first order approximation, a linear relation between the oscillator frequency and the current can be found:

$$f = 1/(2 \cdot N \cdot t_0) = I/(2 \cdot N \cdot C \cdot V_{osc}) . \quad (1)$$

Where f is the oscillation frequency, N the number of inverters in the ring, t_0 the single inverter delay, C the capacitance at each inverter output and V_{OSC} the oscillation voltage swing. Since N, C and V_{OSC} are fixed as soon as the inverters are sized, the current can change the frequency in a direct and linear way.

First the behavior of the ring oscillator by itself has been simulated and it has been noticed that the oscillation frequency was increasing accordingly to the increase of the temperature. That is because the phenomenon of thermal inversion has been observed [17]. Let's take into consideration the simple expression of the current of a transistor in saturation:

$$I = \mu \cdot C_{OX} \cdot W/(2 \cdot L) \cdot (V_{gs} - V_{th})^2 . \quad (2)$$

Where μ is the carrier mobility, C_{OX} the oxide capacitance and V_{th} the threshold voltage. Mobility is known to be decreasing with the increase of the temperature due to lattice vibrations, but in TSMC 65nm CMOS technology V_{th} has also a similar behavior. In the temperature range that interests this sensor application (-30°C ~ 120°C), the current trend is actually dominated by the threshold variation, that can be approximated as:

$$V_{th}(T) = V_{th}(T_0) - K \cdot (T - T_0) . \quad (3)$$

Where T is the actual temperature, T_0 the room one and K the correlating experimental constant [9]. Thus a PTAT current exploiting the same threshold voltage behavior has been designed to feed the ring oscillator and enhance its temperature characteristic. The resistor R is used just to compensate the voltage drop due to the current mirror transistor, in order to obtain an oscillation

symmetrical around half the supply voltage value. A fourth inverter is then added to bring the oscillation to a rail-to-rail swing.

3.2.3 Inaccuracy Model

Since a free-running ring oscillator is used to transform the temperature information into a frequency reference, its phase noise impact on the sensor performance must be accurately analyzed, since it is an intrinsic source of measurement error. Let's consider a TCO frequency behavior like the one showed in the upper right corner of Fig. 28, where F_{max} is the highest frequency that occurs at the highest temperature T_{max}, and F_{min} is the lowest frequency that occurs at the lower temperature T_{min}. This is due to the 65nm TCO having PTAT behavior. In other technology nodes the relation to be considered between temperature and frequency could be reversed. The difference between F_{max} and F_{min} will be called ΔF, while the one between T_{max} and T_{min} will be ΔT. Let's also assume to have a N-bit counter. So the longest possible counting period would be:

$$t = (2^N - 1) / F_{max} . \tag{4}$$

Without considering rounding errors, the extreme values of the counter output will be:

$$N_{max} = F_{max} \cdot t , \tag{5}$$

$$N_{min} = F_{min} \cdot t . \tag{6}$$

Now with a simple operation the resolution of the sensor can be estimated as:

$$\text{Resolution} = \frac{T_{max} - T_{min}}{N_{max} - N_{min}} = \frac{\Delta T}{\Delta F \cdot t} = \frac{F_{max} \cdot \Delta T}{(2^N - 1) \cdot \Delta F} . \tag{7}$$

From (7) it can be seen how to improve the sensor resolution: increasing the number of bits of the counter; having a steep slope of the TCO frequency characteristic; having a low maximum frequency. The first two options are expected, while the last is because with a lower maximum frequency the counter can have a longer active period in order to enhance the differences between two close temperatures.

Now let's consider a phase noise PN (in linear value) obtained at F_{offset} from the main oscillation frequency F. F_{offset} has to be chosen in the region where the white noise sources dominate the 1/f noise in the oscillator, where the phase noise displays a -20dB/dec slope. For a free-run ring oscillator a simple accumulating jitter can be considered. From [18] the single period jitter can be computed as:

$$J = \sqrt{PN(T) \cdot F_{offset}^2 / F^3} . \tag{8}$$

During the counting period t, there are $F \cdot t$ oscillation periods. So, from (8), the k-cycle or long term jitter J_k, where k is the number of periods, can be found as:

$$J_k = \sqrt{k} \cdot J = \sqrt{(2^N - 1) \cdot PN(T) \cdot F_{offset}^2 / (F^2 \cdot F_{max})} . \tag{9}$$

If bigger than a single oscillation period t_{period}, that jitter is going to change the counter output code with an error of as many least significant bits (LSBs) as

$$LSB_{err} = J_k / t_{period} = J_k \cdot F = \sqrt{(2^N - 1) \cdot PN(T) \cdot F_{offset}^2 / F_{max}} \,. \tag{10}$$

From (10) it can be observed how the error on the output counter is dependent of the temperature. Since the region of phase noise that is taken into consideration is due to thermal noise, the error will increase if the temperature increases. At the same time, increasing the number of bits of the counter or having a low maximum frequency worsen the LSB error. That seems in conflict with the resolution performance showed in (7), but it happens because each LSB would represent a smaller temperature step.

Multiplying (7) with (10), the actual temperature inaccuracy or error of the sensor can be calculated:

$$Inaccuracy = Resolution \cdot LSB_{err} = \frac{\Delta T}{\Delta F} \cdot \sqrt{PN(T) \cdot F_{offset}^2 \cdot F_{max} / (2^N - 1)} \,. \tag{11}$$

The one-sigma inaccuracy computed in (11) is just due to the free-run oscillator phase noise. So it is intrinsic to that kind of system and cannot be eliminated. Since that is a value that is going to be placed on top of the usual sensor calibration inaccuracy, it has to be taken into consideration during the design phase, because it could become a major source of error. Thus some observations have to be done in order to obtain a guideline to mitigate its effects:

- it increases with the increase of the temperature, because of the phase noise behavior;
- a steep slope of the frequency characteristic curve ($\Delta F/\Delta T$) improves the accuracy;
- a higher number of bits on the counter decreases the inaccuracy;
- a low maximum frequency is more desirable, keeping a constant ΔF.

Another possible way to get rid of that intrinsic error is to get several measurements and average them, before obtaining the final temperature value. But that is at the expense of a lower data rate and a higher energy consumption for the final measurement.

3.2.4 Design Validation

To validate the analytical model, a Matlab Simulink model performing a transient analysis of the sensor system has been built. Since the phase noise taken into consideration is due to the white noise in the ring oscillator, it has been modeled as a normal distribution Gaussian random variable with zero mean and $\sigma = 1$. The system has been built assuming the parameters reported in Table 1. They have been chosen to be similar to the ones achieved by our system, but with a worsened phase noise performance in order to emphasize its impact on the sensor inaccuracy and better observe the model behavior. Analytically, an inaccuracy on single measurement of ±3°C has been calculated using (11). The Simulink model results are shown in Fig. 29. The solid lines represent the limits established by the analytical results.

Table 1. System Parameters

ΔT	120 °C
ΔF	200 MHz
F_{max}	1 GHz
F	500 MHz
PN	-60 dBc/Hz
F_{offset}	10 MHz
N	12

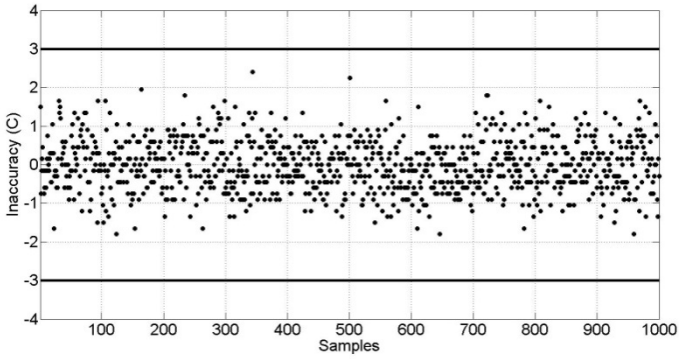


Figure 29: Inaccuracy Model Analytical Result (Solid Lines) versus Simulink System Model Results

It can be immediately seen how all the samples fall well inside the expected interval. So the analytical model provides a good worst case estimation of the ring oscillator phase noise effect on the sensor inaccuracy in case of single measurement.

3.3 Close-loop TC-LNA Design

The gain of the 94GHz LNA can be tuned in two ways. The first is changing the bias of the common source transistor of the second stage between 375mV and 550mV, in steps of 25mV. The second is changing the number of active multipliers of the common source transistor of the second stage. Knowing that, the temperature compensation procedure has to follow these steps:

1. Create the compensation look-up table (LUT) containing the LNA bias setting for each temperature (Table 2).
2. Perform a 2-point calibration across temperature of the temperature sensor output. Fig. 30 shows the TCO output frequency versus temperature for different process corners.
3. Find the equation of the corresponding calibration line on the output of the asynchronous counter: $N = m \cdot T + q$. Fig. 31 shows the behavior of the counter output when its input is enabled.
4. The compensation logic reverses the line equation and calculates the temperature from the value of the temperature sensor output: $T = (N - q)/m$.
5. The compensation logic sets the correspondent LNA bias setting looking in the compensation table.

Following the procedure that has just been described. The LNA gain has been compensated to just 1dB variation across the wide temperature range -40°C ~ 120°C. Fig. 32 shows how the gain variation without compensation was more than 4dB. At the same time the NF of the LNA remains almost untouched (Fig. 33), because it is mostly set by the LNA first stage.

Table 2. LNA Temperature Compensation Table

Tmin (°C)	Tmax (°C)	Vbias2 (mV)	EN (V)
-40	-30	375	1
-30	-20	375	1
-20	-10	375	1
-10	0	375	1
0	10	400	1
10	20	400	1
20	30	375	0
30	40	425	1
40	50	425	1
50	60	400	0
60	70	450	1
70	80	425	0
80	90	450	0
90	100	525	1
100	110	550	1
110	120	550	0

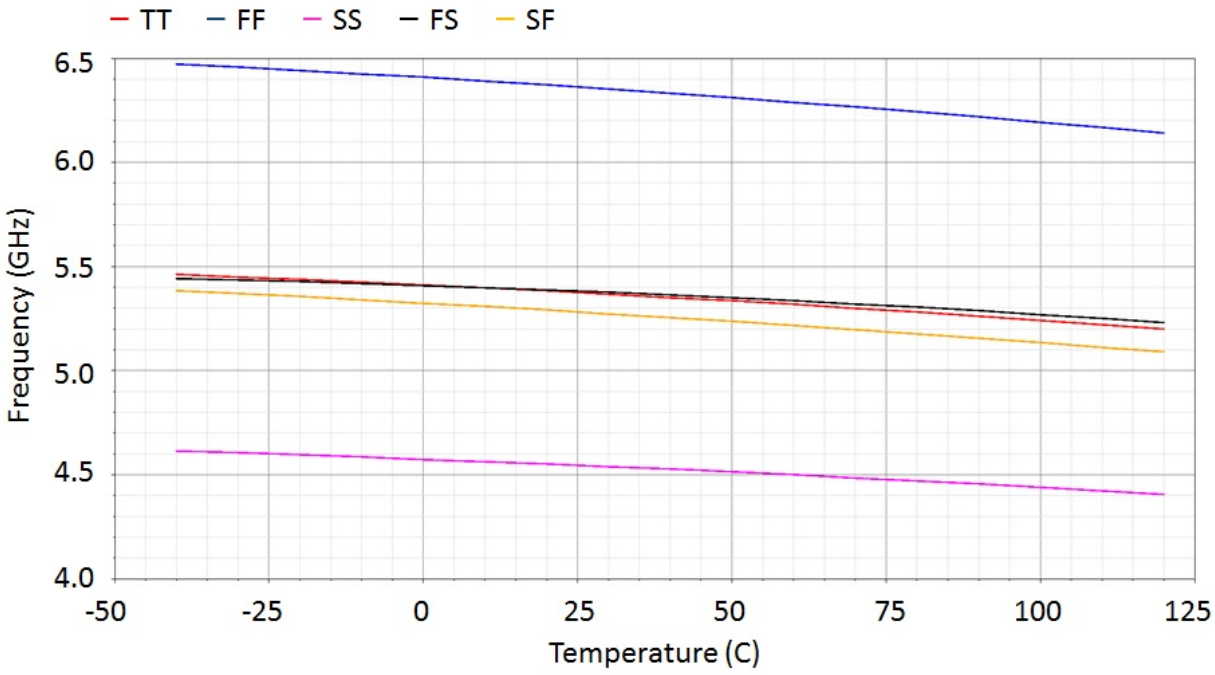


Figure 30: TCO Output Frequency versus Temperature across Process Corners

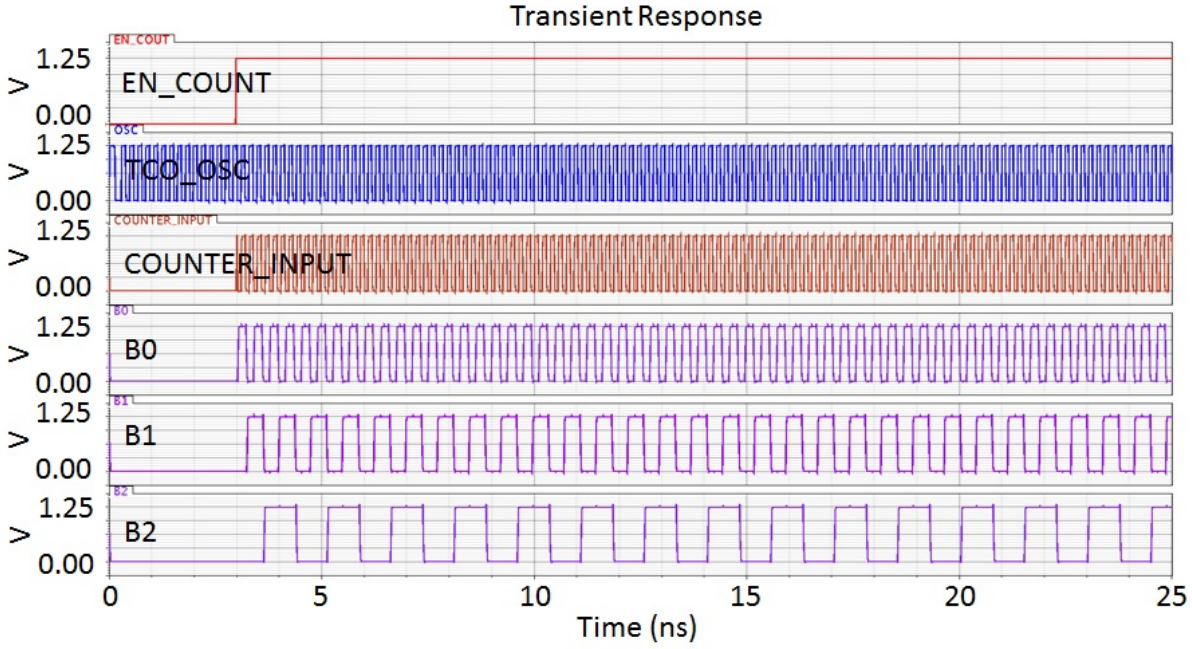


Figure 31: Counter Output over Time

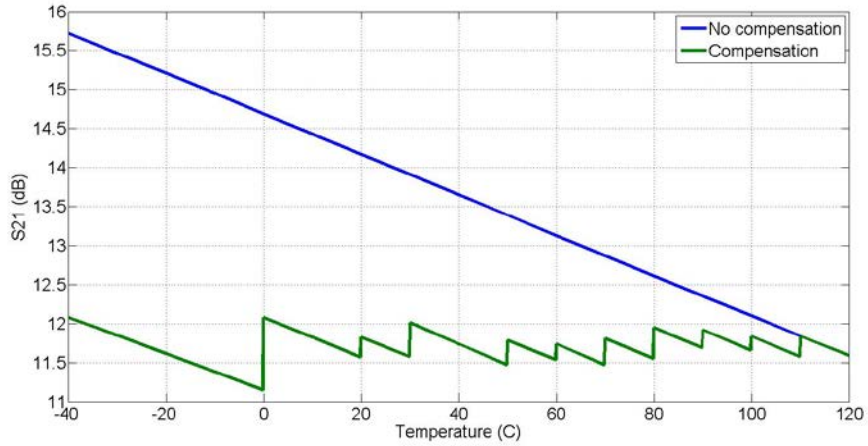


Figure 32: LNA Gain over Temperature without (Blue) and with (Green) Compensation

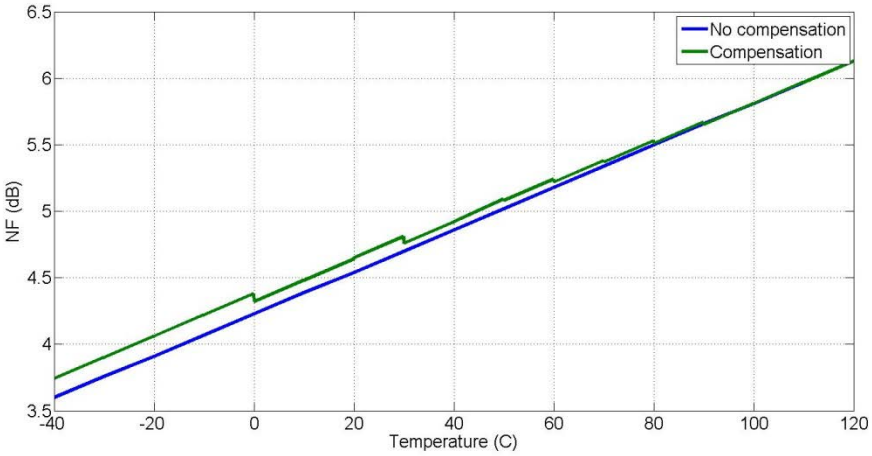


Figure 33: LNA NF over Temperature without (Blue) and with (Green) Compensation

3.4 Noise Figure Measurement Results

W-Band (75-110 GHz) monolithic microwave/millimeter-wave integrated circuits (MMICs) are rapidly maturing. In general these circuits are tested in W-Band waveguide test fixtures where radiations (signals) from a W-Band wave guide is coupled to a microstrip line and/or to a coplanar wave guide then the MMIC. This testing approach of W-Band MMIC has several drawbacks; it can be costly due to waveguides and test fixtures involved and not suitable for high volume testing. It suffers from repeatability due to the assembly involved and bonding ribbons affecting the accuracy for the correction of the transition.

W-Band on wafer probe stations are now common in millimeter-wave testing labs. The W-Band noise figure measurement system configuration we have developed can be used in an existing probe station set up and can be easily extended for automated W-Band on–wafer noise figure measurements as well as for the capability to accommodate noise figure measurement of in-fixture MMICs and devices.

3.4.1 Noise Figure Measurement System Configuration

The developed noise figure system is based on the theory of the noise figure measurement [19-21]. It is similar to the one applied to the lower frequency test systems. A block diagram is shown in Fig. 34 and its principle is based on the Y-Factor method. In designing the above mentioned noise figure measurement system, all critical components affecting accuracy and repeatability were carefully chosen. The main components of this noise system configuration are: a frequency multiplier, a low noise amplifier, a W-Band mixer, isolators, noise source and WR10/1mm coax adapters. An external signal generator is used as the input signal to the frequency multiplier and a spectrum analyzer is used for power data collection.

An active four times Quinstar frequency multiplier is used, it takes its input from an external analogue signal generator that has a frequency range capability from 18.75 to 27.5 GHz to produce a full W-Band bandwidth after multiplication. Isolators are used in appropriate places in the system chain to minimize the mismatch uncertainties.

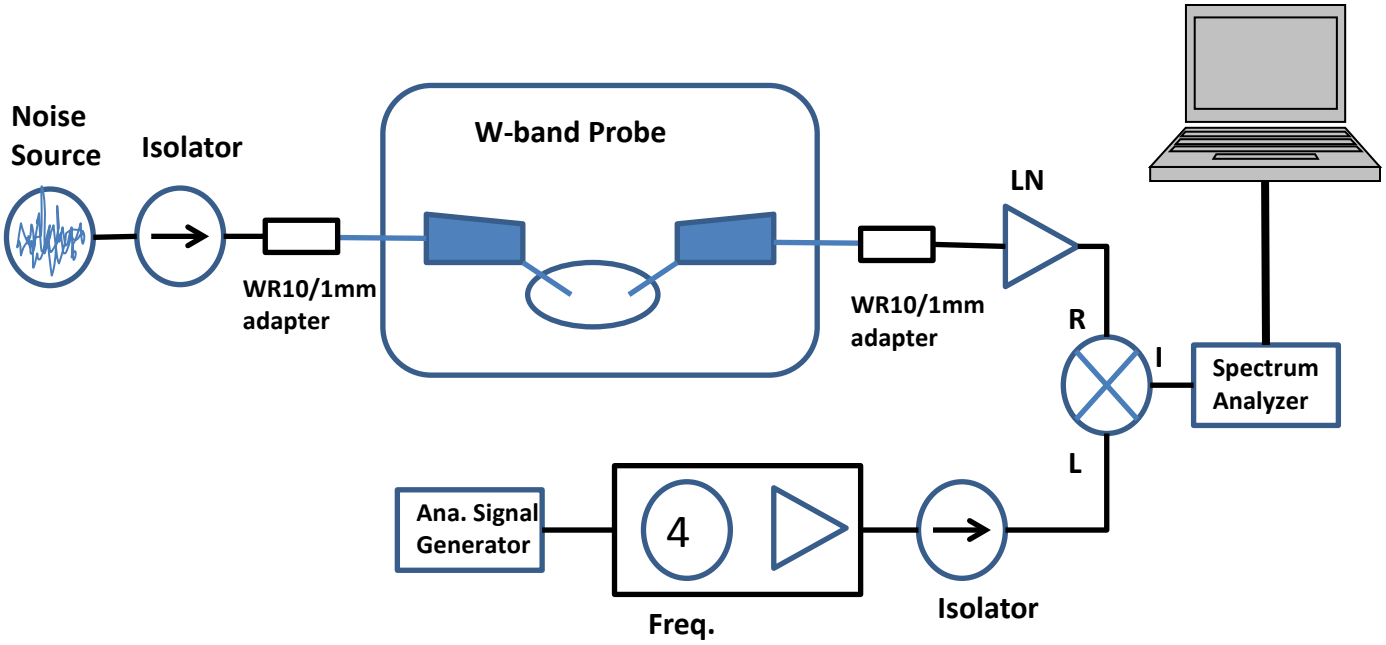


Figure 34: W-Band Noise Figure Measurement System

One of the most critical components in this noise figure measurement system is the noise source. It needs to generate an adequate noise level such that the power difference when switching between the hot and cold state is high. A noise source that has an excess noise ratio (ENR) of 15 dB is used. Its ENR is sufficient enough to handle the reduction or loss contributed by the isolator, waveguide/cable and the RF probe.

A low noise amplifier is placed after the device under test (DUT) and before the mixer to reduce the system noise and provide sufficient signal gain to be input to the RF port of the mixer. The used LNA is a "Quinstar" QLW-75B05522 that has a W-Band operating range. It has 5.5 dB Noise Figure and 22 dB of gain. The main purpose of this LNA is to increase the signal level such that the system noise is not degraded by the conversion loss of the mixer.

The mixer used is also "Quinstar" made; it is a fixtured double balanced mixer that has WR10 wave guide flange pattern for the RF and local oscillator (LO) ports where as the intermediate frequency (IF) port (low frequency port) is a subminiature version A (SMA) connector. The required LO levels is specified to be between 11 dBm minimum and 17 dBm maximum with 13 dBm nominal. For the prescribed power levels the expected conversion loss is 7.5 dB for an IF band of 5 GHz.

3.4.2 Test and Preliminary Results

To verify functionality, initial tests were carried out without the probe station and with the rest of the components assembled as shown in Fig. 35. The purpose of this initial test is to make sure the frequency multiplier, as well as the down conversion are properly functioning.

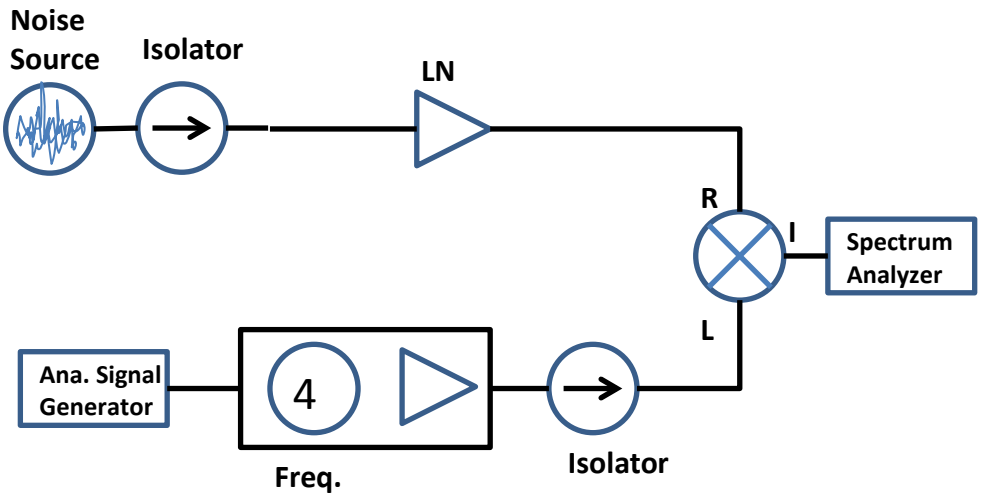
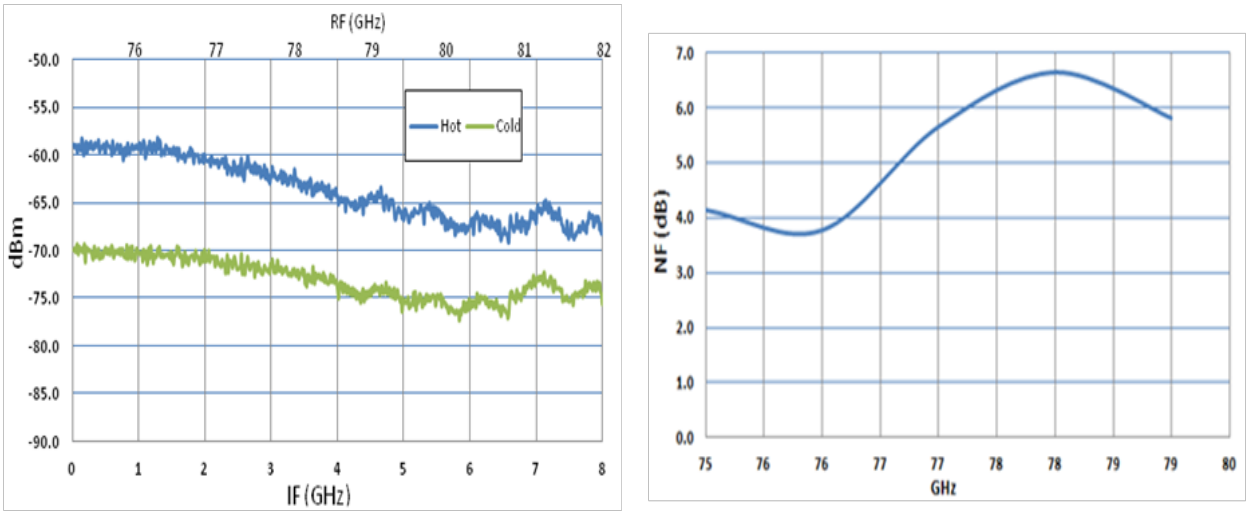


Figure 35: W-Band Down Converter Test Setup

The method of measuring noise figure in this set up is the Y-Factor method that is used behind the scenes in noise figure meters and analyzers. It involves applying a noise source to DUT input and taking measurement of noise power at the output. The Y-Factor is defined as the ratio of "hot" (noise source is ON) to "cold" (noise source is OFF) measured noise power . The noise figure of a DUT is then computed using the specified/calibrated noise source ENR values following the formula:

$$NF(\text{dB}) = 10\log10(F) = ENR(\text{dB}) - 10\log10(Y\text{-}1). \quad (12)$$

Fig. 36a, shows two measurements for the low side of W-Band, where the LO frequency is 75 GHz after multiplication by 4 of signal generator input. The two plots represent the power measured at the spectrum analyzer when the noise source is "hot" and "cold", these are the two measurements that are necessary to compute the Y-Factor and noise figure. Although the LNA is an integral part of this noise system configuration, in this set up it can be seen as a DUT for validation of the overall test setup. The computed noise figure is shown in Fig. 36b and matches closely the published noise figure of the LNA. The valid RF frequency range for this particular measurement is 75-80 GHz since the used mixer bandwidth is 0 to 5GHz, so the remaining W-band frequency range is accomplished by increasing the LO frequency.



(a) **(b)**

Figure 36: W-Band Down Converter Measurement (a) Hot, Cold (b) Computed NF

3.4.3 Measurement, Characterization and Troubleshooting of two Low Noise Amplifier

As mentioned earlier in the tasks description, two distinct low noise amplifiers designed to operate at 94 GHz were characterized in terms of their behavior, such as bias conditions and scattering parameters. Measured results were used to establish how well active as well as passive models for the two used processes compare to measured results. The processes under consideration are the IBM 45nm silicon process and the COSMOS (under R&D) where the device material used is an indium phosphide (InP) heterojunction bipolar transistor (HBT).

For the IBM 45nm silicon process a one stage LNA, a two stage LNA, and various passive components in the die shown in Fig. 3, were measured and compared to simulated results. The discrepancies between measured and simulated performance were identified and a few attempts were implemented to externally tune the LNA. Measured data reports were submitted to concerned party.

The second characterized LNA uses COMOS InP HBT process, also expected to operate at 94 GHz. Issues in the design process were identified. They are mainly large variation from one circuit to the next in the same vicinity, large discrepancy between the simulated and needed bias to get the simulated gain and a shift in the input match that is most likely due to models of the passive components used. Capacitors used within the chip as well as the ESD circuit protection functionality were isolated tested (Fig. 38). A full report of findings in form of a presentation and generated data was submitted to the primary investigator.

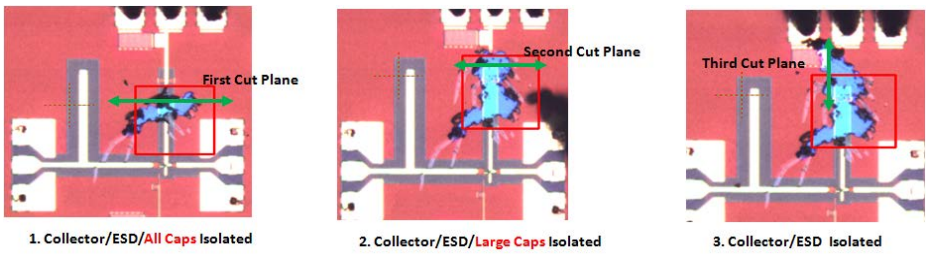


Figure 37: Characterized COSMOS 94 GHz One Stage LNA

4 CONCLUSIONS

The simulation and measurement results successfully met the research objectives. This project focused on discovering techniques to build wide temperature range electronics for millimeter wave imaging applications. Realization of this plan has resulted in a comprehensive body of work that systematically addresses the device, circuit and compensation algorithm aspects of millimeter wave imaging. The research has significant intellectual merit which will affect multiple science and engineering disciplines. The research and education objectives are closely integrated, and the work has significant broader impacts to Air Force technology capabilities and millimeter wave electronics in general.

5 RECOMMENDATIONS

Based on the analysis of the current study the following recommendations for future work are offered.

5.1 Recommendation 1: Complete the TC-LNA Design in 45nm SOI CMOS

The first tape-out gave us many data points for the individual transistor, capacitor, and transmission line. To put the temperature sensor and the 94GHz LNA together, it is necessary to perform another tape-out. Fig. 39 shows the proposed complete block diagram. Together with the mm-wave fixture, this circuit can be made as a plug-in module directly useful for Department of Defense (DoD) missions.

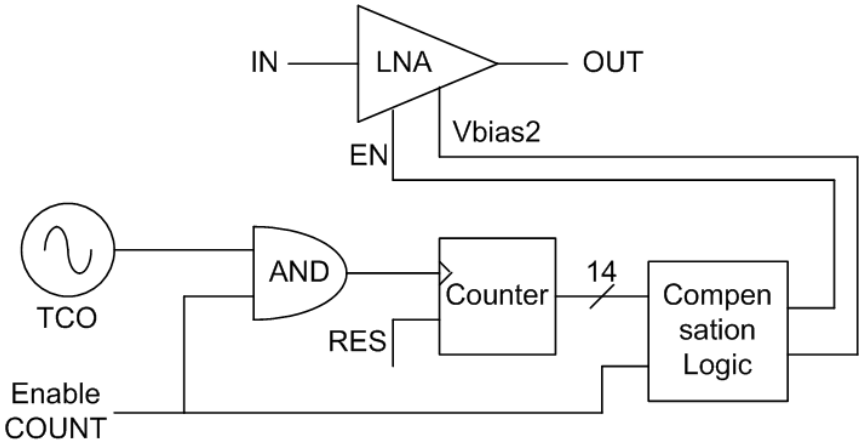


Figure 38: Complete Block Diagram of a 94 GHz Temperature Compensated LNA

5.2 Recommendation 2: Improve the Testing of TC-LNA by Designing and Manufacturing a mm-wave Test Fixture

Accurate characterization of MMIC and solid state devices is limited by metrological techniques due to increased parasitics, smaller physical dimensions and the interfacing method used. Typically at millimeter-waves, MMICs whether packaged or in a die form, eventually must be mounted on a fixture that provides a way to connect the chip or an assembled module to the test equipment such a network analyzer, spectrum analyzer, antennas etc. Millimeter-wave fixtures introduce substantial insertion losses and return loss, if they are not handled properly, they will mask the true performance of the DUT. Calibration is usually done at the network analyzer with known standards. A DUT in the fixture measurement reference plane is removed from the physical device terminals by the fixture geometry. The discrepancies caused by the shift in the reference planes are removed/compensated for using known de-embedding technique. The intent of this task is a design of a W-Band test fixture (with a potential to be used as fixture module) that is wide band, that is repeatable and has the necessary transition performance such as coax to microstrip optimized in terms of insertion loss and return loss. Three coax millimeter wave connectors will add the capability of the fixture to handle three port chips/networks such as mixers and receivers/transmitters. The fixture would also have feed thru pin for DC biasing. An illustration is shown in Fig. 40.

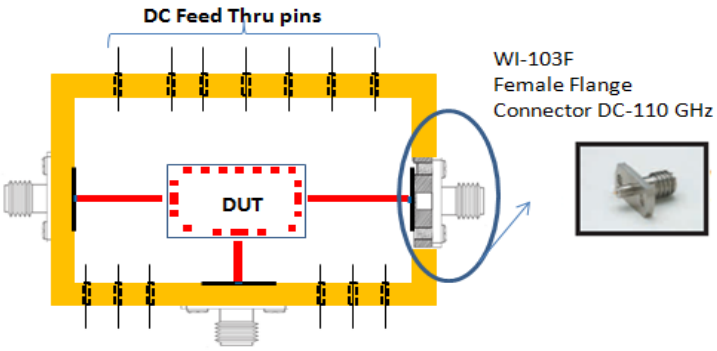


Figure 39: Three Ports W-Band Test Fixture

5.2.1 Background and Technical Approach

To date coaxial connectors have evolved significantly, advances include K (2.92 mm), 2.4 mm, and V (1.85 mm) connectors that pushed the upper frequency to 60 GHz. Furthermore the 1 mm connector/launcher operating mode-free up to 110 GHz are now off the shelf available components. Rectangular wave guides such as WR10 (W-Band) to 1 mm coax connectors are also readily available. In this design we intend to use 1 mm coax launcher shown in figure 6 in at least two of the three ports. While most equipment used for high frequency circuit measurements such as network analyzer and spectrum analyzers use coaxial structures for signal inputs and outputs, microstrip line is used as planar transmission line for millimeter wave circuits. Therefore coaxial to microstrip transmission is required. One millimeter flange-mount such as the one shown in Fig. 40 is selected for this design.

Traditionally the coaxial cable to microstrip transmission, a common feature of microwave systems and in microstrip test fixtures, is accomplished by either using the standard touchdown contact or use of an optimized forehead contact. Because of simplicity, cost, fabrication ease and flexibility, a touchdown contact is investigated for this design.

Although the impedance between the coaxial and the microstrip line is matched to 50 Ohms, there is a strong electromagnetic field discontinuity between the cylindrical coaxial structure and the rectangular nature of the microstrip line. The fringing fields over the launch region make the transmission capacitive in nature, exacerbating field matching issues especially at millimeter-wave frequencies. Calibration procedures can remedy the insertion loss introduced by the transition, however maximum power transfer is still needed, and thus an optimized return loss.

Various techniques have been used to improve high frequency performance of the coaxial to microstrip transmission, they are mainly three:

1) By tapering the inner and outer conductors of the coax connector so that the distance between conductors decreases linearly and the outer conductor ends just at the level of ground plane of the dielectric substrate (Fig. 41a) [22]. Another tapering method involves gradual lowering of the central pin in such a way that transforms the coaxial field distribution to a microstrip distribution [23].

2) Providing a compensation gap by inserting a hole below the inner conductor of the coax extended pin near the transition by drilling the ground plane and the lower mechanical structure

(Fig. 41b) [24]. The return loss can be optimized by adjusting the vertical and the horizontal of the air gap. This has the effect of reducing the inherent capacitance produced by the transition and fields dispersion.

3) By adding inductive notches to the microstrip line close to transition point (Fig. 41c).

All these three methods have produced good results at moderate to high frequency. The first two methods do however have customized high fabrication cost. We elected to use the third option based on fabrication cost and also the flexibility to use wider types and sizes of microstrip lines.

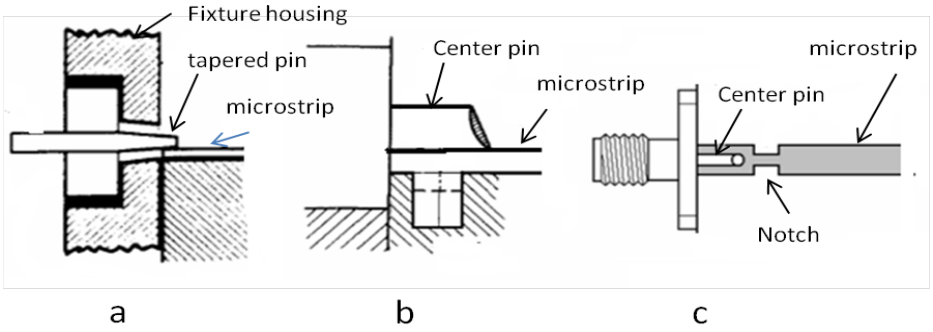


Figure 40: Coaxial to Microstrip Line Transition Improvement Types

Another critical component that is affecting the fixture performance is the choice of the substrate used in the transmission line. It is well known that a transmission line should have a thinner substrate and high permittivity so that the signal is confined to the dielectric and free of spurious radiations. Thicker substrates are more inductive and produce intrinsic radiations that distort matching characteristics. Even though high permittivity is required for the signal to propagate properly, high permittivity will cause high signal attenuation, less efficiency and narrow bandwidth. Substrate properties also influence transmission line dimensions satisfying 50 Ohms impedance. The microstrip line is narrower for thinner substrate and high permittivity. Alumina substrate was chosen for its manufacturability, good dielectric properties, and relatively good thermal properties and mechanical characteristics.

5.2.2 Preliminary Simulation Results

For the performance evaluation and design criteria improvements of the proposed test fixture, we are using full 3D electromagnetic simulator HFSS software. A Software program that is highly accurate and it has the capability to solve electromagnetic field for complex structures.

The coaxial connector characteristics used to implement the coaxial to microstrip transmission are those of Anritsu W1-103 female flange mount connector (shown in Fig. 42) that has a frequency range of from DC to 110GHz, 50 Ohm impedance, a 0.7dB Insertion loss and typical 1.38 VSWR (S11~16dB). As for the microstrip line substrate we are using alumina that has a 9.8 dielectric constant and a 0.0005 loss tangent.

The full model structure shown in Fig. 43 will undergo a full three dimensional (3-D) electromagnetic (EM) simulation to establish a base line s-parameter performance evaluation.

Then a notch will be introduced in the transmission line (Fig. 43c) and its dimensions will be optimized to give the best performance.

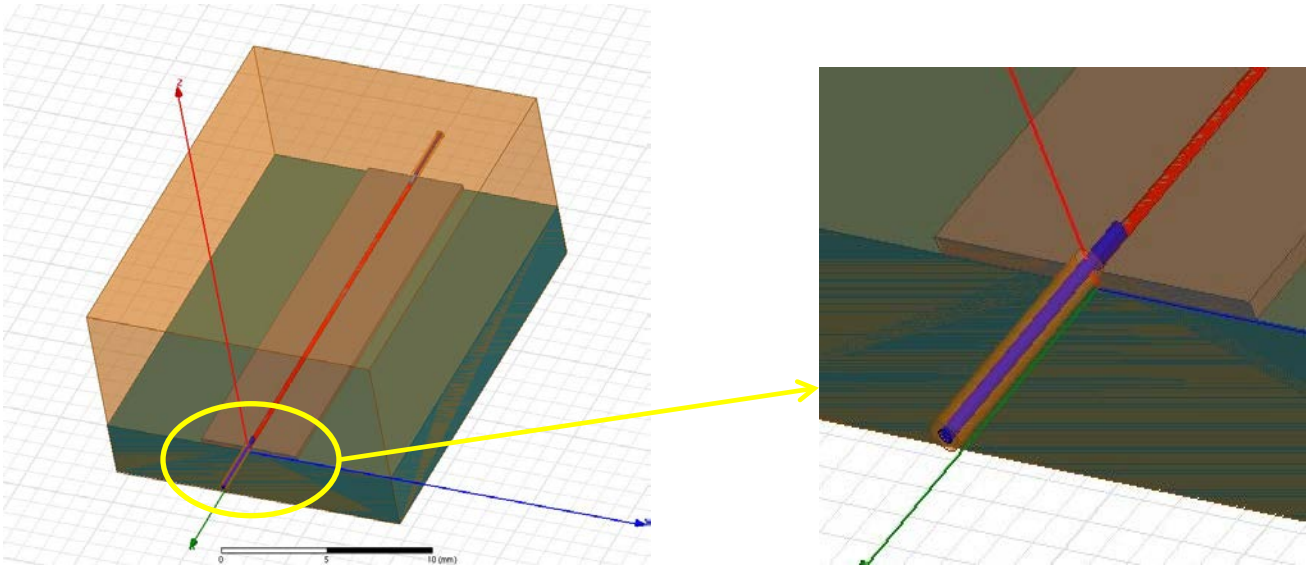


Figure 41: W-Band 3D Fixture Model

However before performing a full electromagnetic simulation and solving the fields for the whole structure, the two main components of the fixture namely the 50 Ohm microstrip line and the 1mm coax connector were simulated separately. This serves a few purposes: to make sure that the proper mode (transverse electromagnetic) is propagating through, that the impedance is correct across the band, and obtained simulated results will provide a base line and insight on the upper limit performance for when the whole fixture is simulated. Simulated results for the coax connector and the microstrip are shown in Fig. 43 and Fig. 44, respectively.

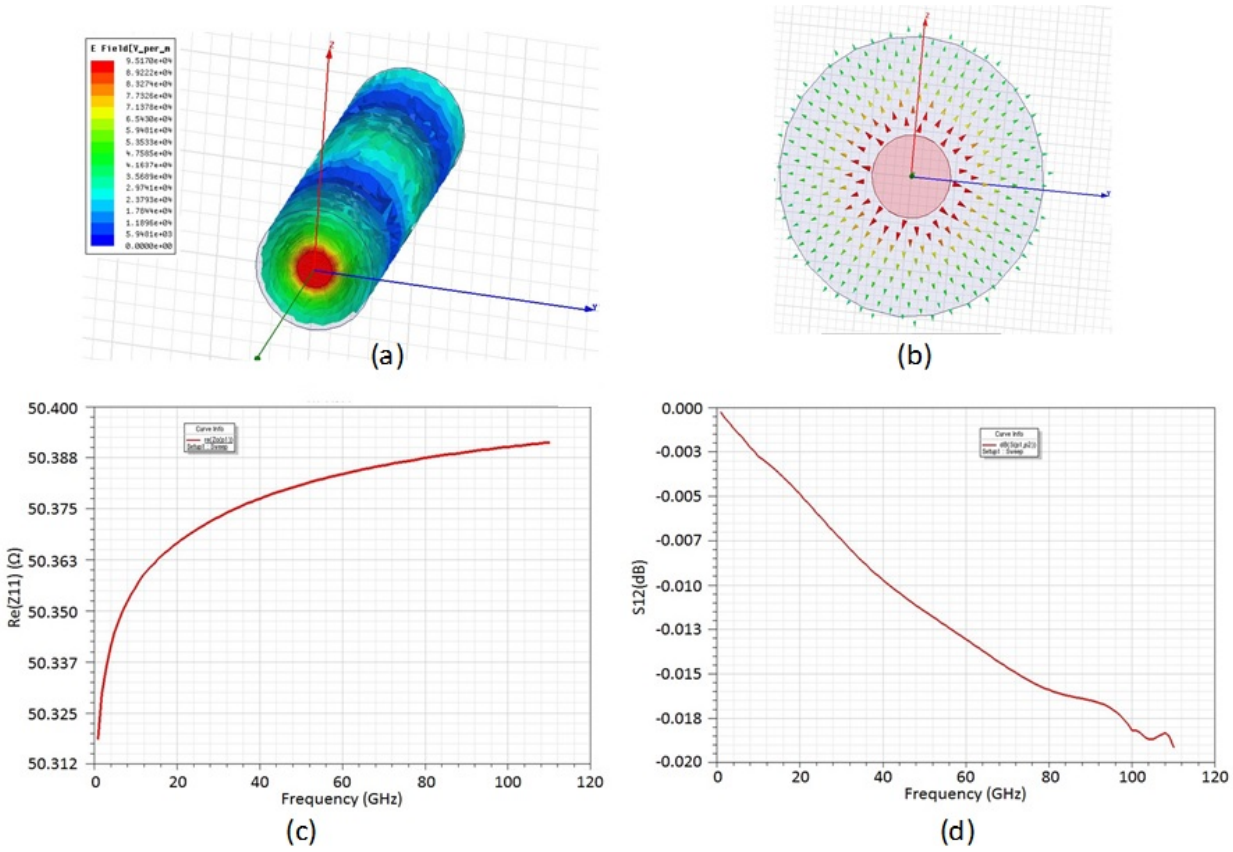


Figure 42: 1mm Coax Connector 3D EM Model Simulation
(a) radiation plot (b) input port cross-section vector fields plot (c) impedance plot (d) insertion loss plot

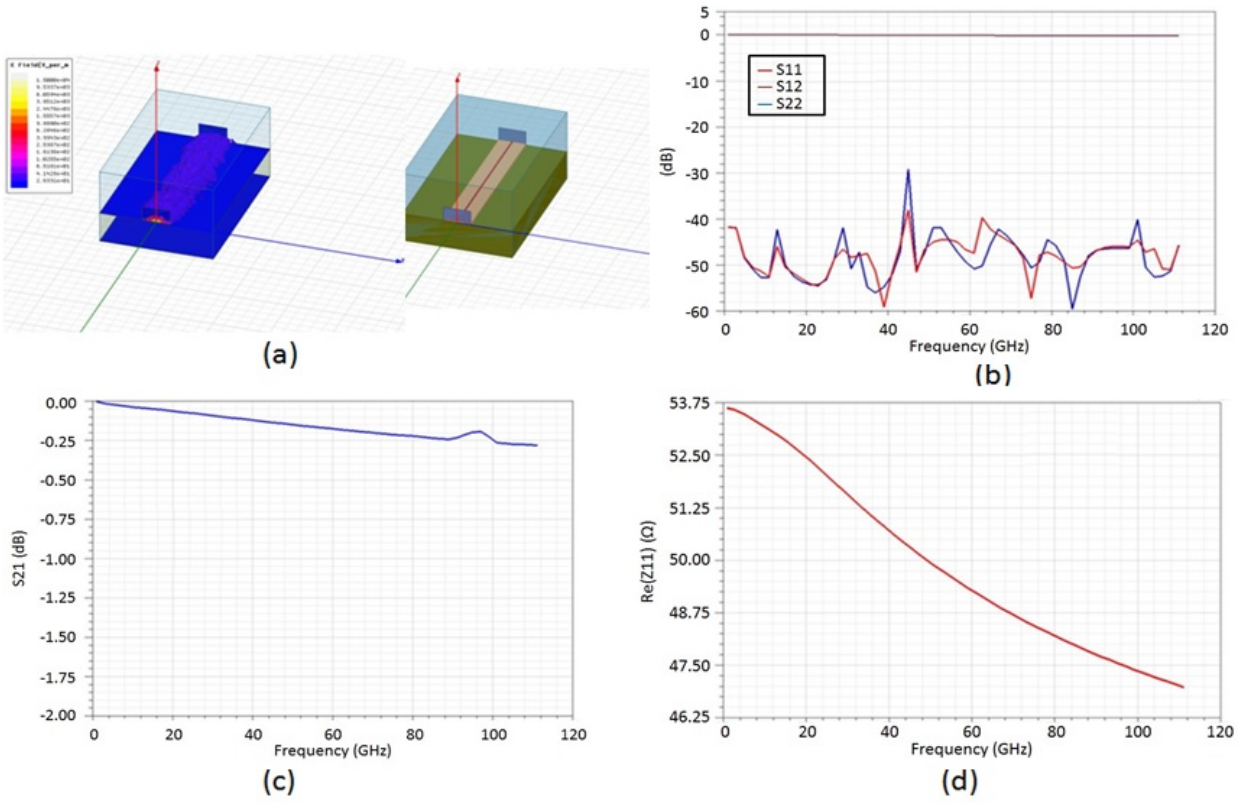


Figure 43: Alumina 50 Ohm Microstrip 3D EM Model Simulation
(a) radiation plot and model (b) s-parameters (c) insertion loss (d) impedance

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LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS

ACRONYM	DESCRIPTION
3-D	three dimensional
AFRL	Air Force Research Laboratory
BJT	bipolar junction transistor
CMOS	complementary metal-oxide-semiconductor
COSMOS	compound semiconductor materials on silicon
CPW	coplanar waveguides
CS	compound semiconductor
DARPA	Defense Advanced Research Projects Agency
DC	direct current
DoD	Department of Defense
DUT	device under test
EM	Electromagnetic
ENR	excess noise ratio
ESD	electrostatic discharge
GND	ground
GSG	ground-signal-ground
HBT	heterojunction bipolar transistor
HDMI	high-definition multimedia interface
IEEE	Institute of Electrical and Electronics Engineers
IF	intermediate frequency
InP	indium phosphide
ISQED	International Symposium of Quality Electronics Design
LNA	Low Noise Amplifier
LO	local oscillator
LSB	least significant bitpage
LUT	look-up table
MMIC	monolithic microwave/millimeter-wave integrated circuit
MOSFET	metal-oxide-semiconductor field-effect transistor
NAECON	National Aerospace & Electronics Conference
NF	noise figure
NMOS	N-type metal-oxide-semiconductor
PDK	process design kit
PI	principal investigator
PTAT	proportional to absolute temperature
RF	radio frequency
RTD	resistance temperature device
SiGe	silicon germanium
SMA	subminiature version A
SOI	silicon on insulator
TC	temperature compensated
TCO	temperature controlled oscillator

ACRONYM	DESCRIPTION
VLSI	very-large-scale integration
$\square_{DR}$	dutch roll frequency
°	degree